

Oruga

Data Acq with DSP co-processor
64 Input 16-bit up to 66kSPS each
4 DAC 16-bit up to 2MSPS each
Super flexible triggering

Features

- 225MHz TMS320C6713 DSP
- Advanced DMA and cache controller
- 32MB Memory
- 64 Analog Inputs, up to 66kHz/ea muxed 32:1 into two 16-bit A/Ds (32 inputs capable of 130kHz/ea)
- 4 D/A 16-bit to 1MHz each (optional)
- Complex trigger modes
- Multi-board Synchronization and Triggering

Applications

- High-channel Count Data Acquisition
- Capture and Real Time Co-processing
- High-end Desktop Data Logging
- Test and Measurement
- Vibration/Acoustic Monitoring & Analysis
- Industrial Control

Hardware Options

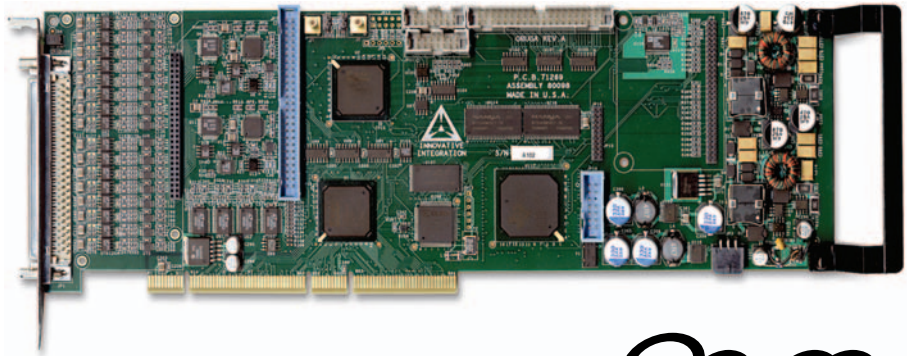
- IO Cable and terminal block
- JTAG Debugger
- FIFOPort Cable
- SyncLink/ClockLink cable

Software Development Tools

- Pismo Toolset for Oruga
- TI Code Composer Studio

Ordering Information

Oruga-32 (32 input chs, No DAC)	80098-0
Oruga-32D (32 input chs + 4 D/A)	80098-1
Oruga-64 (64 input chs, No DAC)	81002-0
Oruga-64D (64 input chs + 4 D/A)	81003-0



Oruga

Overview

Oruga is an intelligent PCI data acquisition/playback card capable of capturing 64 analog input channels with 16-bit resolution at 66 kSamples/second each, and playing 4 analog output channels at up to 1MSamples/s, with advanced triggering options offering an amazing flexibility. The C6713 DSP assures the control of all peripherals and offers ample math co-processing bandwidth with extreme flexibility and ease of programming. With a very complete set of peripherals for a fast system integration, including digital I/O, private external data port and multi-board synchronization, Oruga is a complete solution for desktop and industrial PC applications requiring high-channel count high-resolution data acquisition/playback and optional co-processing: test and measurement, data logging/playback, OEM instruments, acoustic and vibration analysis, industrial control.

Description

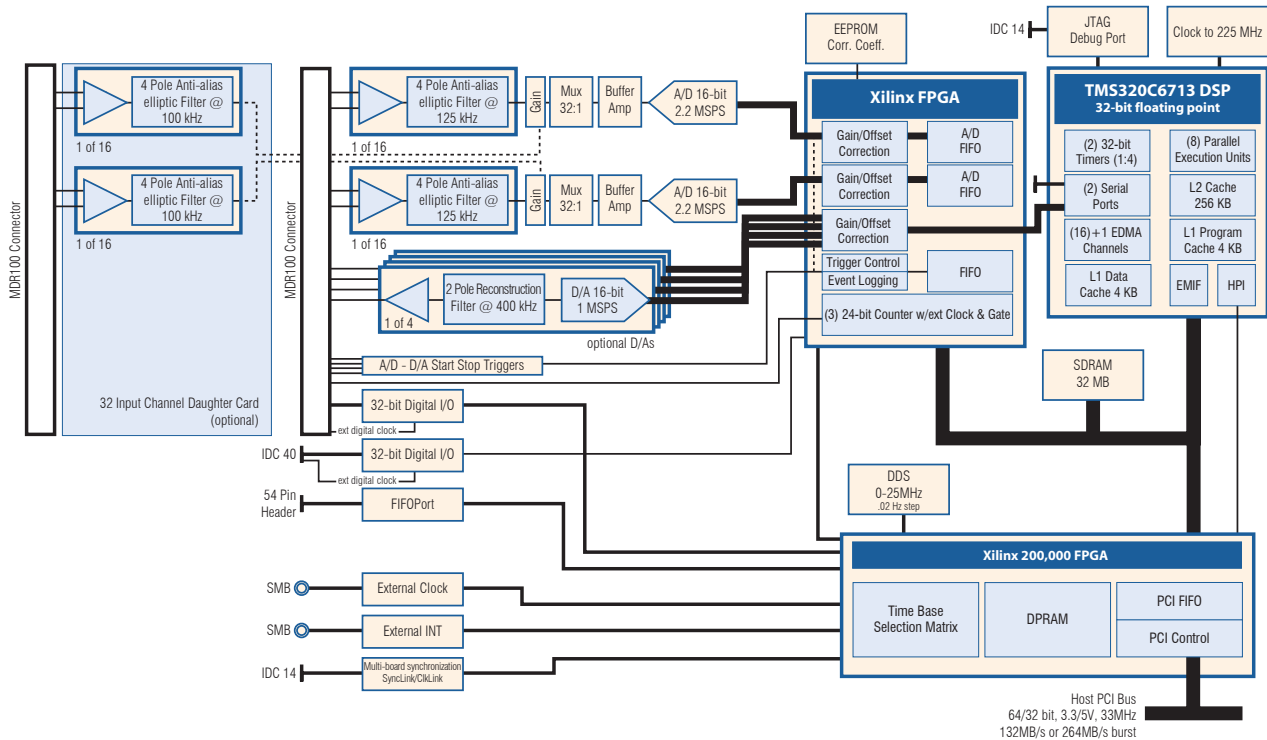
The analog front-end consists of 64 independent input channels and individual anti-alias filters, arranged in two banks and multiplexed 32:1 into two 2.2MSPS A/D converters. The control logic offers a wide selection of triggering modes and clock sources, all configurable in software and allowing one to configure any type of complex acquisition scheme. A decimation mode also supports two concurrent streams, one at high-speed and one at low speed, for optimum utilization of bus and CPU bandwidth as well as host CPU and disk logging capacity. The four independent 1MSPS D/A output channels also benefit from this advanced trigger control and offer high-end analog performance for agile, flexible waveform generation, playback or closed loop controls. Simultaneous four-channel-playback can sustain 750 KSPS per channel.

The TMS320C6713 is Texas Instruments fastest floating point DSP, utilizing all strength and maturity of the C6000 series. With 256KB of on-chip memory, an efficient two-level cache controller and 16 DMA channels, the C6713 is recognized by developers as the most "C-friendly" processor. Oruga's software libraries make good use of DSP/BIOS peripheral drivers to facilitate end-user code development for the most complex multi-thread applications while optimizing bandwidth utilization. The toolset includes turn-key data acquisition and playback application with source code that illustrates the best utilization of all hardware resources.

Oruga is a 64bit/33MHz PCI card supporting 264MB/s burst busmastering operation from/to host PC memory, but is also compatible with 32-bit PCI bus. A parallel interrupt-driven communication channel supports 16 mailbox-type message channels for command and control functions with the host application. The board also presents numerous features for a smooth system integration: 64 bits of general purpose digital I/O, a fast bi-directional external data FIFOPort, and a SyncLink/ClockLink port for easy multi-board or external hardware synchronization.

DSP Processing Core and On-Board Resources

Oruga is powered by one TMS320C6713 Digital Signal Processor clocked at 150MHz, Texas Instruments' fastest 32-bit floating-point DSP. It uses an efficient two-level cache architecture, with L1 cache of 4KBytes of data and 4kBytes of program and a large 256Kbytes that can be partitioned via software setup between L2 cache and unified mapped RAM. The enhanced DMA controller handles 16 independent channels, which greatly relieves the CPU for bulk data movement. The EMIF is interfaced via two Xilinx logic devices to the A/D channels, digital IO



and PCI interface. One of the two multi-channel serial port (McBSP) is controlling and feeding data to the DAC channels. The second McBSP is pinned-out for the end-user. The 16-bit HPI port is used for booting purposes and accessed via the on-board PCI interface. There are two 32-bit timers on-chip.

On-board resource include 32MB SDRAM, three 24-bit timers, one DDS 0-25MHz timebase, and a screaming-fast 32- or 64-bit, 33MHz PCI interface with FIFO buffering. One Xilinx logic chip controls the analog converters, start/stop trigger signals and 32-bit DIO. The firmware includes FIFO buffering of A/D data, digital gain/offset correction and decimation of the low speed channels. A second Xilinx device handles the PCI interface, the timebase selection matrix, the FIFOport interface and the other 32-bit DIO port.

A real-time alert queue in the firmware allows the DSP programmer to log -and later read- specific hardware events like start and stop triggers, data integrity flags and user-defined events with hardware precision. The alert message timebase is driven by a 10MHz 40-bit counter. All these features are implemented in logic and can therefore evolve or be extended or customized to support new applications. The firmware can be upgraded in the field under DSP software control, using a “Burn” program provided in the software tool set.

Analog Input Channels

Oruga presents 64 single-ended or differential input channels with a +-10V range arranged in two banks of 32 channels each. The input ranges can be customized for each individual channel via software, with a maximum of +-10V. Inputs are DC-coupled and maximum input signal bandwidth is 100kHz. Each input signal is fed through a 4-pole Sallen-Key filter set at 100kHz that can be by-passed via jumper and connected to a buffer amplifier, upstream of the 32:1 multiplexer, so that settling transients and “channel smearing” are eliminated. Each multiplexer output is connected to one AD7621 16-bit 2.2MSPS converter with 1 LSB non-linearity and AC performance with SFDR above 85dB. Oruga has an auto-calibration feature using software-controlled switch and on-board reference voltages that allow end-users to calibrate the card in the system without removing external wiring.

The two A/D converters can use a separate timebase so that end-users can configure a mix of high-speed and low-speed channels. For the high-speed stream, the trigger timebase signals can be selected from several clock sources: on-board DDS, DSP timers, logic timers, external clock, a SyncLink/ClockLink pin or software command. The selection is made via software commands. When configuring one bank of channels as a low-speed stream, the timebase can be selected from the following choices: high-speed timebase divided by N (16-bit divisor), software or external clock.

Oruga also provides incredible triggering flexibility, that is fully software configurable. The data capture is defined with start and stop signals that basically apply a mask -or gate- condition to the timebase clock signal. The start trigger can be selected from a wide choice of signals: timers, external interrupt, SyncLink/ ClockLink pin, software command or analog threshold. The Stop time is also flexible and allows different modes of operation: specific duration using a timer, specific length as defined by number of samples acquired, or other signals like external interrupt, SyncLink/ClockLink pin or software command. Once can easily configure the system for repeated framed acquisitions based on hardware or software event.

The 64-channel Oruga consists of two boards, the main PCI board and a daughter board. The base board features 32 A/D channels split in to two banks of 16. Each bank of 16 is fed into a mux and an A/D converter, allowing each channel to operate at nearly 130KSPS. The optional daughter card integrates an additional set of 32 input channels that are combined with the baseboard's standard input upstream in the same fashion. This daughter board consumes one adjacent PCI slot and provides its own MDR100 signal connector.

Analog Output Channels

Oruga offers an optional four D/A channels at 16-bit resolution with sampling rate of 0-1MHz each, using Linear Tech LTC1597 converters. The standard output ranges are set at $\pm 10V$ but can be customized with resistor changes. Each DAC output is connected to a 2-pole Sallen-Key smoothing filter set at 400kHz and output signals are DC-coupled. Similar to the A/D operation, the D/A triggering is extremely flexible both in terms of timebase clock source and start/stop signaling. The D/A timebase and start/stop trigger signals can be different from the A/D control. The board allows in-system auto-calibration of the D/A through the A/D, completely under software control. D/A channels are interfaced to the DSP with one McBSP port at 50 Mbit/s maximum supporting the four channel mode at 750 KSPS per channel. All D/A channels are on the baseboard.

Standard Peripherals for Fast System Integration

Oruga is more than a high-performance data acq or real-time processing board. With a complete set of system-level features, Oruga is a fast deployment solution for professional systems in industrial and OEM applications. Standard peripherals include:

- 64-bit of general purpose digital I/O, split in two banks of 32-bits (TTL)
- External Data FIFO Port allowing 50MB/s bi-directional data transfer to/from external hardware on 16-bit wide port
- External clock and interrupt input connectors (50-ohm coax)
- External start/stop trigger signal input (TTL)
- SyncLink/ClockLink connector for multi-board or external hardware synchronization (TTL and LVDS)

The SyncLink/ClockLink feature allows developers to synchronize multiple boards in a system. It provides up to six unique timing signals and event triggers to be shared between up to 16 cards. Each Oruga card has a switch matrix that routes any event trigger to any SyncLink/ClockLink port, completely under software control. There is no complex cabling, just a simple ribbon connection and software configuration.

The DDS module provides an agile digital timebase that can drive analog conversion but can also serve as a transmit strobe, as a timer/counter signaling DSP interrupts, or as a timebase to clock external hardware. The DDS source itself can be chosen between on-board crystal oscillator, SyncLink/ClockLink, external interrupt or external clock.

The PCI interface is implemented in firmware, which greatly relieves the DSP load. It features a 64-bit bus interface capable of busmastering data bursts up to 264 MBytes/sec. The interface can accommodate 64bit/32bit and 3.3V/5V buses running at 33MHz and configures itself to the host bus configuration at power-up. The PCI interface manages all busmaster and messaging activities, independent of the DSP, and greatly simplifies the integration of Oruga in Windows host applications. Software layers provide a full messaging sub-channel system for command and control using an arbitrated 256-word dual-port RAM. Sixteen different message channels can be individually steered to the desired application thread, and each message can include a command word plus 14 words of data. With mailbox style messaging, the DSP and host can exchange status and data structure with minimum interference on each other.

DSP Development Tools

The Oruga development pack contains all the necessary hardware and software to start and complete a new development project. It includes the Oruga card, Code Composer Studio integrated development environment from Texas Instruments for the C6000 series DSP, a JTAG emulator, I/O cabling, and the Pismo toolset for Oruga.

Innovative Integration's Pismo toolset makes DSP development fast and simple with a complete collection of target and host side libraries. It includes everything from convenient utility applets for download, execution and high level debugging of DSP applications to a complete set of source code with examples demonstrating the full operation of Oruga at full bandwidth. The Pismo toolset is fully integrated in Code Composer Studio. Pismo supports and extends each of the features of DSP/BIOS on Oruga through a seamless integration of advanced C++ class libraries, BIOS-compliant DSP peripheral device drivers and clear, illustrative examples. On-line help files support the software programmer during development and also serves as a good learning tool.

Communication with the host application utilizes two modes of data transfer: bus-mastering initiated by the DSP for bulk data movement in both directions, and up to 16 message channels, initiated by either the DSP or the host, with interrupt support, for lower bandwidth command-and-control type of handshakes. The Pismo PCI drivers and message classes make it simple to create and utilize these communication channels on both target and host sides.

Host side development is supported with Innovative Integration's Armada toolset. This set of tools is integrated into either Borland C++ Builder or Microsoft Visual C++ and offers the most powerful and flexible means to rapidly integrate real time digital signal processing into Windows applications. Armada allows development of simple yet powerful application programs capable of exploiting the full power of Oruga including efficient data movement synchronized with target code, viewing/graphing, signal post-processing or analysis, and disk logging. Host side example programs are also provided and clearly illustrate data and message passing as well as data post-processing.

OEM Configuration

Oruga can be configured to fit specific requirements, including custom firmware or hardware. Contact Innovative Integration with your specific OEM requirements.

Digital Signal Processor

Texas Instruments TMS320C6713 DSP
 225MHz
 32-bit Floating-point DSP
 4KBytes L1 Data Cache
 4KBytes L1 Program Cache
 256KB partitionable between L2 cache & PRAM
 Two 32-bit timers
 16 EDMA channels
 Two McBSP (sync serial ports)

Memory

32MB SDRAM (1wait-state)
 256word dual-port RAM for host message exchange

FPGA

Xilinx Spartan-II for I/O and trigger control
 Xilinx Spartan-II for PCI interface and FIFOPort

PCI Interface

Logic core in Xilinx chip
 32/64bit 3.3/5V 33MHz
 Controller auto-detects host bus type
 Busmaster or target operation
 Busmaster burst rate to 264MB/s (on 64-bit)
 HPI used for bootstrapping and mailbox communications
 512x32 FIFO for busmastering
 256word RAM for mailbox messaging

FIFOPort

External data port
 16-bit wide in each direction, TTL interface
 LVDS driver supported with add-on FIFO cable
 50+ MBytes/sec rate in each direction
 256x32 FIFO receiving buffer

Timers/Counters

Two 32-bit timers on DSP
 Three 24-bit timers in logic
 Input clock is on-board 80MHz crystal or
 External Clock or SyncLink/ClockLink input

Analog Input

32 or 64 channels, single-ended or differential,
 DC-coupled split in two banks of 32 and
 multiplexed 32:1 into two 16-bit A/D converters
 AD7621
 Sampling rate: up to 66kS/s on all 64 channels
 or higher sampling rate for a lower channel count
 Max Input bandwidth 100kHz (op amp response)
 Input range software programmable $\pm 10V$, $\pm 5V$,
 $\pm 1V$, 0-10V
 4-pole Sallen-Key Anti-alias filter set at 100kHz
 on each input (jumper can by-pass)
 Digital gain and offset calibration in logic with
 coefficients stored in ROM
 Dual 512x32 sample FIFOs
 400MB/s burst rate to DSP

Analog Output (optional)

4 channels, 1MHz each, 16-bit
 using LTC1597 D/A converters
 Output signal is DC-coupled
 Output range $\pm 10V$ (individually customizable
 with resistor change)
 Output reconstruction filter 2-pole Sallen-Key set
 at 400kHz (customizable with resistor change)
 Digital gain and offset calibration in logic with
 coefficients stored in ROM
 Factory calibrated
 McBSP used as interface between DACs and
 DSP 50Mbits/sec aggregate data rate (i.e. 750
 KSPS per channel when using all four DACs)

Digital I/O

64-bit, distributed in two 32-bit ports
 Programmable as input or output in groups of 8
 TTL compatible with $\pm 24mA$ capability

Time Bases and Trigger Methods

DSP and logic Timers
 Programmable DDS 0-25MHZ in 0.02Hz steps
 External Clock
 SyncLink/ClockLink input signal (TTL or LVDS)

Multi-Card Synchronization

SyncLink/ClockLink shares up to
 6 signals (5TTL+1LVDS) between boards and/or
 external hardware to synchronize timebase
 and/or trigger event signals

Connectors

Two 100 pin MDR connectors for analog I/O
 50 pin shrouded polarized male IDC for digital I/O
 & start/stop trigger
 40 pin shrouded polarized male IDC for user DIO
 14 pin shrouded polarized male IDC for SyncLink/
 ClockLink
 14 pin shrouded polarized male IDC for JTAG
 54-pin header for FIFOPort
 SMB for external clock and Interrupt

Physical Size

PCI – Full size (32-bit and 64-bit bus
 compatible)
 Single width for 32 channels
 Double width for 64 channels

Power Requirements

To be determined

Development Languages

DSP: C or assembler using CCStudio and Pismo
 toolkit
 Host: MS VisualC++ or Borland C++ Builder

DSP Operating System

DSP/BIOS II

Host system Operating System

Win2000 / WinXP

Software Selection Guide for Oruga

Software Package	Description	Usage/Requirements	Page	Notes
Pismo Toolset	Peripheral libraries needed for developing code on this card. Includes host applications and target examples in source form demonstrating use of peripherals on the card, DSP/BIOS peripheral device drivers.	Requires CCStudio* Windows2000/XP compatible.	98	Required for all first time users. Includes technical support.
Caliente DLL	Dynamic link library (DLL) for the Oruga.	Requires ANSI-compliant C/C++ compiler. For example, Microsoft Visual C/C++. Windows2000/XP compatible.		Required for interfacing Host side code to DSP. May be used without Armada although not recommended
CCStudio 'C6000	Integrated development environment (IDE) for Target side development/debugging from Texas Instruments.	Requires XDS-510 compatible JTAG emulator for debugging capabilities.	91	Required for all first time users. Recommend use with Innovative Integration plug-n-play PCI JTAG emulator.
Armada	Host side development package using a revolutionary integrated development environment (IDE). Allows user to build/debug sophisticated data acq apps fully using MS Windows graphical environment quickly with Innovative Integration's Visual Component Libraries (VCL) or MFC Classes.	Requires Borland C++ Builder* or Microsoft Visual C++.	103	Included in Pismo Toolset. Offers easiest interface while providing the most flexibility and performance. Ties into a plethora of 3rd party components.

The Oruga Development Package contains all software packages listed above.

*Contact Innovative Integration for current release version.