

UWB PMC/XMC I/O Module

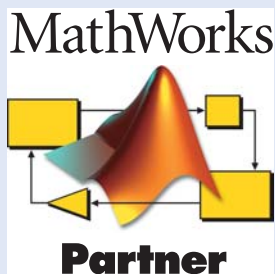
2 Ch. Ultra-Wide-Band Receiver
250 MSPS A/Ds
Large FPGA for User Code
Deep memory

Features

- Two LTC2242-12, 12-bit 250MSPS converters
- 300MHz analog input bandwidth
- Support for undersampling applications
- Virtex-II Pro FPGA, 4 Million gates
- PCI 64/66 with Pn4 port to host card
- XMC - 800MB/s full duplex rates per VITA 42
- 64MB SDRAM plus 2MB RAM for FPGA
- Sample clocks: dual external or on-card PLL
- Advanced SW and firmware demo programs using VHDL or MATLAB Simulink

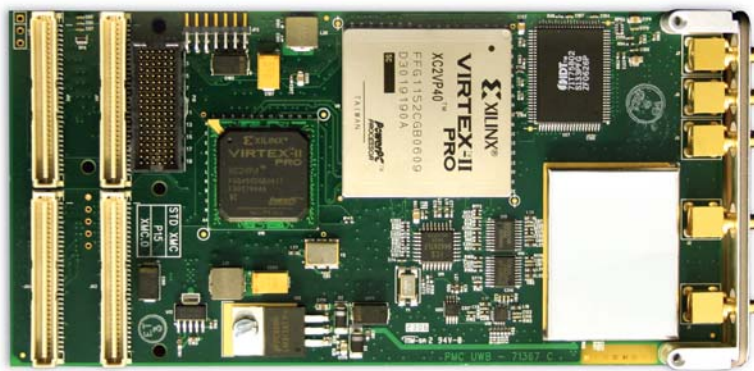
Applications

- Software Defined Radio (SDR)
- Signal Identification
- Electronic Warfare
- Advanced RADAR
- Hardware Testing
- Telecom IP development



Ordering Information

UWB PMC Module 80144-2



Overview

The UWB Receiver PMC/XMC card features the most advanced architecture for ultra-fast signal capture and real-time processing in wide-band radio systems and similar wide spectrum applications. It integrates two 250 MSPS with 300 MHz analog input bandwidth, 12-bit A/D channels with a large FPGA for user-code, ample memory and flexible clocks/triggers on a PMC/XMC mezzanine format. The UWB has Xilinx VirtexII Pro FPGA for signal processing that may be quickly customized using Innovative's Framework Logic in VHDL or in the MATLAB Simulink graphical environment. Large on-card memories for data capture and analysis, a flexible clocking structure, and 800 MB/s connectivity to host DSP cards make the UWB a powerful front end to many applications.

Description

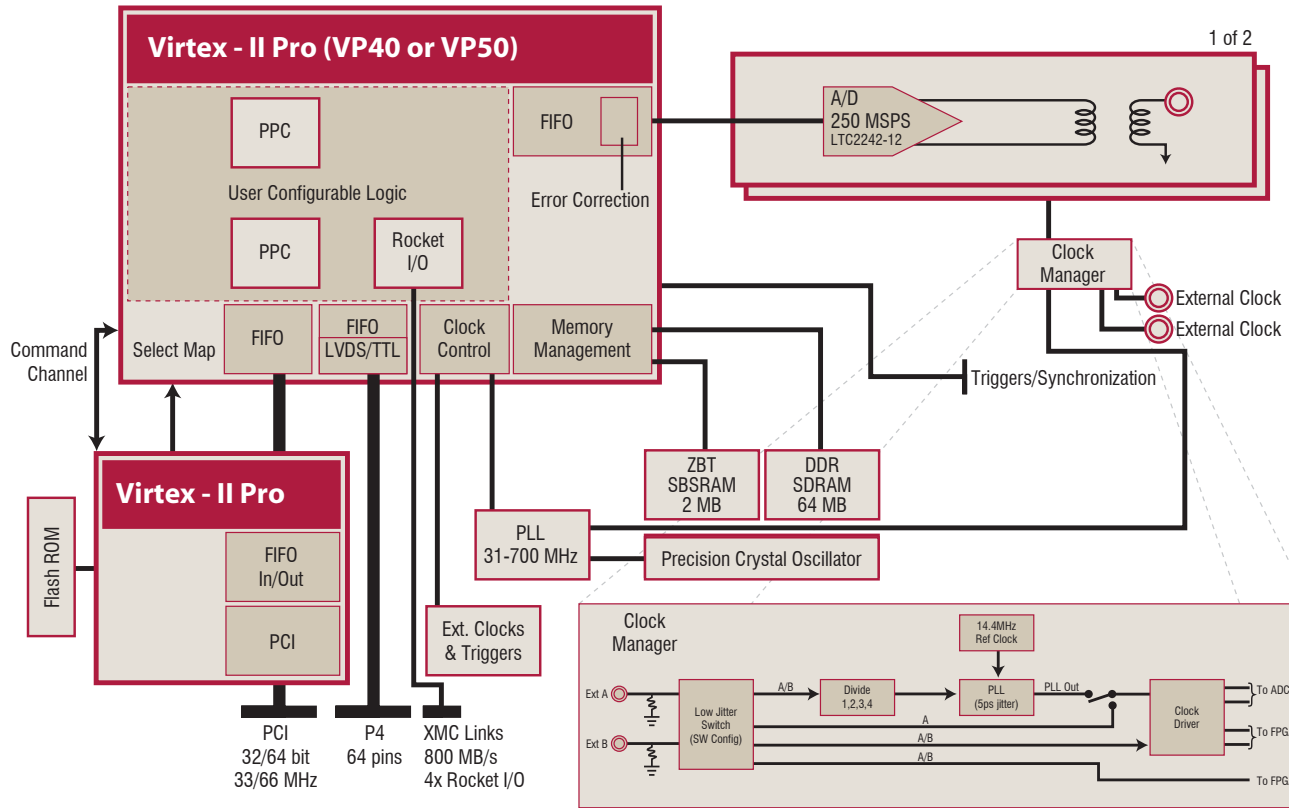
The front-end features two analog input channels consisting of a 50-ohm single-ended input with wide analog input bandwidth characterized to 1 GHz for undersampling applications followed by Linear Technology's LTC2242-12 converter. The A/D data flows directly to the FPGA for processing. The sample rate clock may be selected from one of two external clock inputs or from the on-card PLL. The external clocks may be used directly as a sample clock or divided down and used as a PLL reference. The on-board PLL timebase provides a low-jitter, flexible conversion clock that is programmable by the FPGA. The on-board time base is a highly accurate PLL device ranging from 31MHz to 700MHz with a 3 pico-second maximum RMS jitter. Alternatively, the user can provide individual external clock for each channel, using 50 Ohm SMB inputs. The external clock may be used as a PLL reference.

The UWB Receiver PMC card shares a common architecture with 64MB DRAM buffer memory, and XMC and J4 connection for private data path Innovative's Velocia DSP cards or other host cards. This include a large user-FPGA with dedicated SBSRAM, a PCI-FPGA with large global RAM and private port over PMC connector J4 to the select host cards, such as Innovative Integration's Velocia family. The XMC connection to the host card, with four 2 Gbps full duplex lanes, provides 800 MB/s connectivity.

Ample logic resources allow for flexible integration of the most demanding signal processing blocks such as down/up conversion, complex filtering, resampling, spreading/despreading and clock recovery. For example, the Xilinx DDC logic core for GSM consumes only about 2% of the logic and 1 multiplier. (VP30 and VP50 can be ordered as options)

The application-FPGA controls the I/O, the PLL time base, triggers, 64MB of DDR SDRAM for large data buffering, and a dedicated 2MB SBSRAM. The large 64MB DDR SDRAM memory is available to the FPGA as a data buffer or for use by the PowerPC processors. The Framework logic shows an example of using the memory as a very large FIFO for the data channels. The SBSRAM provides the FPGA with an efficient memory for block-oriented processing or for use by the Power PCs. It is usually exploited for block-oriented signal processing like FFT's.

The application FPGA has two high speed data paths to the host card: PMC J4 and XMC serial channels. The PMC J4 is a private connection from the PMC to the host J4 that provides 42 I/O connections, plus 8 IO on J3 unused pins. J4 can provide up to 350 MB/s connectivity to the host card. Innovative Velocia DSP and FPGA processing cards provide direct connection for J4 to the system FPGAs. The XMC connections are 4 full-duplex, 2.0 Gbps (standard logic speed grade, higher speed grade improves performance) Rocket IO serial ports providing up to 800 MB/s connectivity to the host card.



The user-FPGA is tied with two 2Gbps full duplex serial links signaling to a smaller Virtex 2 Pro logic that serves as the PCI interface and controller. The 64/66 PCI interface supports 528MB/s burst transfers and automatically down-selects to 32 bit and/or 33MHz to permit integration on the widest range of cPCI and PCI carriers. An efficient data packet protocol allows the PMC to support multiple targets for busmaster operations, allowing it to integrate easily with data logging controller cards or into more complex multcard applications for distributed processing.

Firmware for the application FPGA can be configured dynamically via SelectMap, controlled over the PCI bus with the turnkey utilities with software source code provided.

Software and Logic Framework – Custom Logic Support

The UWB VelociaPMC offers a 4M gate FPGA for custom code implementation. Innovative Integration provides source code of the logic blocks implemented on the card as delivered and demonstrating hardware functionality: Front-end I/O control such as programmable amp, A/D and receiving FIFOs, as well as PLL time base control, DDR SDRAM control, SBRAM controller, Pn4 interface, XMC interface and interface to the PCI-FPGA.

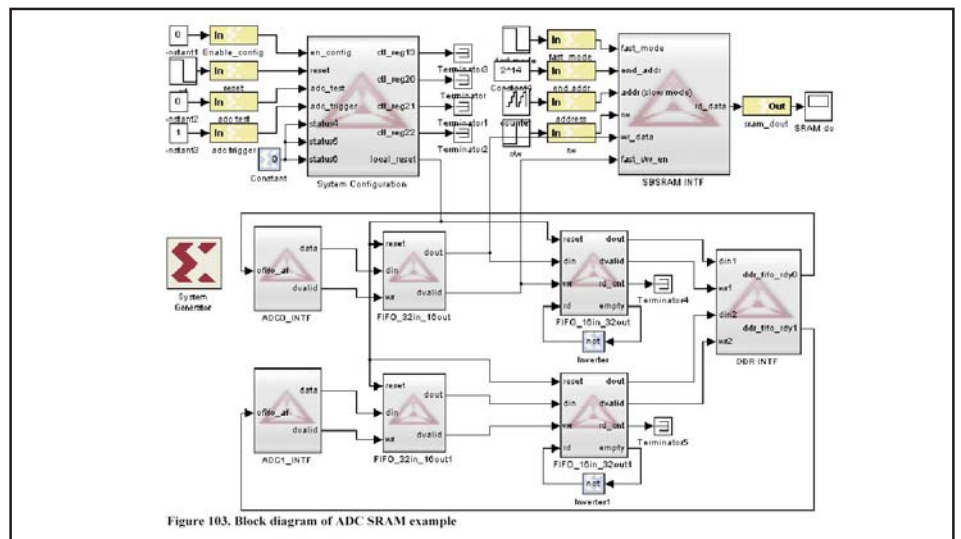
Logic development is supported using VHDL and/or MATLAB. VHDL source files as well as test bench files for ModelSim are provided to customers. The FrameWork Logic provides data

capture from both A/D channels at full rate into a 32MB memory buffer and transfer to the PCI bus interface. Application software provided with the UWB allows the module to log data to disk, illustrating the basic data collection and flow through the module logic.

MATLAB Simulink, in conjunction with Xilinx System Generator may be used for logic development. This powerful graphical tool set allows the signal processing designer to develop algorithms using all the power and grace of MATLAB and then implement them directly in logic. The UWB Board Support Package (BSP)

provides blocks for the hardware interface ready to use in the Simulink graphical design environment. Gateways to MATLAB allow the developer to quickly test the system by using Simulink to generate, analyze and display the actual data on the hardware during design. Nothing could be easier for advanced signal processing development!

Example MATLAB Simulink applications include data logging to disk, using the SRAM for real-time data collection under MATLAB, and hardware-in-the-loop integration of MATLAB Simulink environment with the UWB PMC. These example MATLAB Simulink projects are readily modified



Example of PMC UWB MATLAB BSP

UWB Velocia PMC/XMC I/O Module

to add signal processing using the UWB BSP and Xilinx System Generator under MATLAB Simulink.

The PCI-FPGA is not intended for end-user logic development and source code is usually not provided. Contact Innovative Integration if your application might require changes to these specific interfaces.

MATLAB Examples Illustrating BSP Use

- Capture A/D to SRAM
- Downconversion
- Data acquisition using the DRAM buffer and PCI interface
- SRAM use

Software Support

Innovative Integration's software tool kit for the VelociaPMC series is a powerful collection of software libraries, utilities, examples projects and interactive help file that allow developers to be very productive from the start. Numerous program examples - with source code- demonstrate the usage of every peripheral on the board and provide a framework for further custom development.

Getting started or evaluating the UWB is made easy by using an out-of-the-box application provided with the UWB. This application can flow data snapshots directly to disk for analysis and test, all without any code development, using a standard PC and PMC adapter card.

OEM Configurations

The UWB VelociaPMC board can be configured or modified to fit your specific requirements and provide an optimal mix of performance, cost and features. Contact Innovative Integration with your specific OEM requirements.

Application Information

Application Note: "Multi-channel Software Digital Radio Design Using MATLAB" shows using the UWB with Quadia for a 40 channel receiver.

Input

2 Independent Channels
 50 Ohm Impedance
 Single-ended
 AC Coupled input
 300 MHz analog input bandwidth
 Range +1V to -1V full scale (Other ranges may be custom ordered)
 12-bit A/D Converter LTC2242-12
 Sampling Rate: 40-250 MSPS
 Digital gain/offset correction in logic

Time Base & Triggers

Software selectable timebase : PLL, external input A or B
 PLL reference is 14.4 MHz crystal or external clock A or B divided by 1, 2,4, 8 or 16
 PLL reference clock range: 10 to 25 MHz
 Output Frequency Range: 31 to 700 MHz
 (2) External Clock Inputs, SMB 50 Ohm
 External clock requirements
 800 mV p-p minimum, 0.6 to 1.4V maximum input -0.1V to 3.4V
 External Trigger input, SMB 50 Ohm
 Triggering using external input or software (may be modified in custom logic)
 ICS8751 with 3 ps RMS jitter, Prescaler and M/N type VCO

Application-Configurable Logic

Xilinx Virtex2 Pro XC2VP40-5FF1152C Standard (custom orders supported for VP50 or higher speed grades)
 FPGA Fabric :
 4 Mgate (approx.)
 192 hardware multipliers
 3456 Kb embedded FPGA RAM
 Two PowerPC
 SelectMAP loading from PCI bus
 MatLab Simulink development environment.
 VHDL source code with ModelSim test benches
 JTAG port for download and ChipScope and System Generator
 Pn4 connector 42 pins connect to PMC host (RACE++ pinout)
 Direct connect to XMC - 4 lanes 2 Gbps full duplex
 Logic image is loaded over PCI via SelectMAP interface

PCI-FPGA

Virtex 2 Pro XC2VP4
 Supports PCI interface
 Loads from reprogrammable FLASH memory, in-system programmable

Accessories

BNC to SMB Cable P/N 67021
 PMC to PCI Adapter card P/N 80156

Memory

64 MB DDR SDRAM (call for larger options)
 2 devices configured as 16M x 32 bits, clocked at up to 150 MHz
 Minimum clock rate is 80 MHz
 2 MB ZBT SDRAM organized as 1Mx16 - clock at up to 167 MHz
 Usable either as FPGA memory or PowerPC memory
 Framework Logic provides firmware for DRAM use as FIFO buffer

PCI Interface

64-bit, 66 MHz, 3V
 512 MB/s burst rate
 Packet protocol with credit managed flow control
 Down-selects to 32 bit and 33MHz if needed
 4KB FIFO in each direction

XMC

VITA 42.0 compatible
 4 lanes of Rocket IO
 2 Gbps per lane standard, full duplex
 Directly attached to application FPGA
 800 MB/s aggregate rate, full duplex when using 8b/10b encoding
 Private data path to Velocia DSP and other host cards

Debug Ports

JTAG for FPGA: 14 pin dual row 2mm header compatible with Xilinx cable standard

Connectors

SMB 50 Ohm for analog I/O and Ext Clocks and trigger
 38-pin Mictor connector compatible with many logic analyzer probes (optional)
 Xilinx standard 14 pin header, 2mm for JTAG

Operating Conditions

Forced air cooling is required (1 cubic ft per minute minimum)
 Storage Temperature: -20~80° C (-4~176° F)
 Humidity (Non-operating): 5~95%@60° C (non-condensing)
 Shock: 20 G (operating); 50 G (Non-operating)
 Random vibration: 1.5 Grms (operating), 2.0 Grms (Non-Operating)

Power

Max Power Consumption: 8.4W Typical, 5V @ 0.9A typical, 3.3V @ 1.2A typical, +12V / not used
 (Note: Power consumption is shown for Framework Logic. Power consumption for other logic designs will affect +5V and +3.3V power consumption.)

Development Languages

Logic

VHDL with Xilinx ISE, Mentor Graphics ModelSim, , MATLAB and System Generator
 VelociaPMC Toolset includes libraries, projects, utilities, help files

Host PC

MS Visual C++ , .NET, Borland C++ Builder

Application Software

Data logging and demonstration application (WinXP/2000)

Physicals

IEEE 1386 compliant

Board size

74 x 149 mm (single width PMC size), fits in single slot
 10 mm spacing to host card

Weight

0.11 kg (0.24 lb)

Certifications

CE marked
 EMI and EMC
 Test Report Available

European Standards

EN 55022 Class A
 EN 61000-3-3
 EN 61000-3-2
 EN 55024

Documentation for UWB

Velocia PMC Hardware user Guide
 Framework Logic User Guide
 Malibu Software Development Manual
 MATLAB BSP Manual

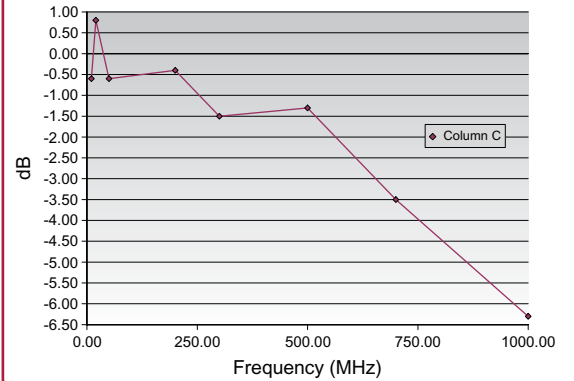
Environmental Data

Lead Free
 ROHS compliant

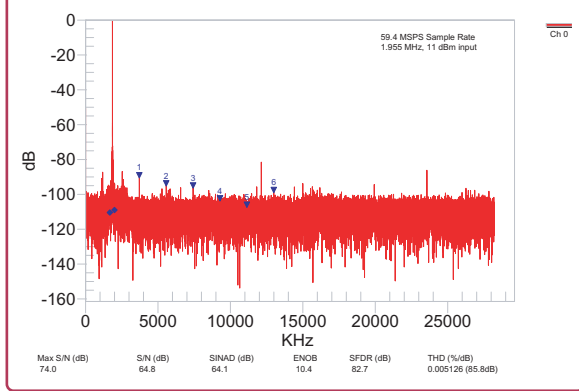
UWB Performance Summary

Parameter	Measured	Units	Test Conditions
DC Accuracy	Offset	Calibrated at factory to <1 bit for average of 50000 samples	Bits 25C, grounded input
	Gain	Calibrated to <0.2	% 25C, Full scale input
AC Performance	ENOB	10.2	Bits 1.955 Mhz input, -1 dBm, 180 MSPS
	SFDR	83	dB, 1.955Mhz input, fs = 180 MSPS
	S/N	65	dB, 1.955Mhz input, fs = 180 MSPS
	THD	-82.4	dB, 1.955Mhz input, fs = 180 MSPS
	Gain Error	<1	dB, 1-500 Mhz sine input, fs = 180 MSPS
Analog Input Bandwidth		-0.9	dB, 300 Mhz
		-2.9	dB, 750 Mhz
		-5.6	dB, 1 GHz
Channel Crosstalk	-83	dB, 250 Mhz sine input	
Power Consumption	8	W	Typical for 130 MSPS 90% logic usage

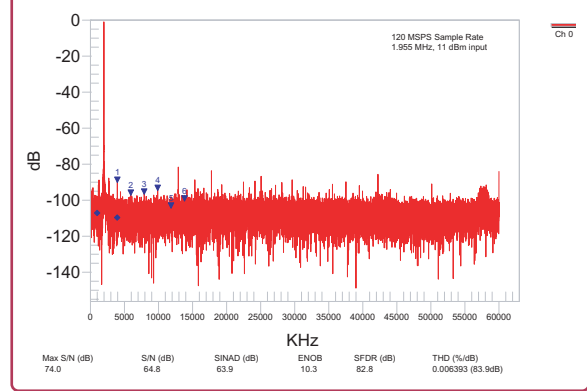
Analog Input Frequency Response



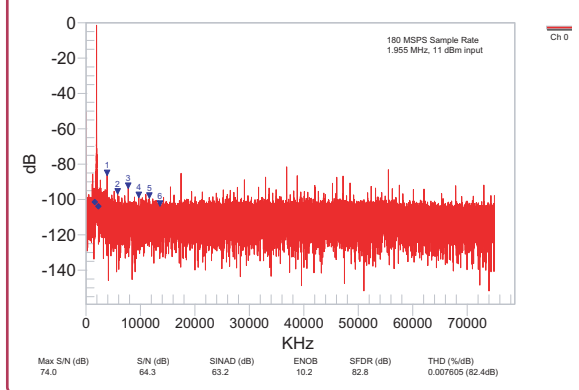
Spectral Response, 59.4 MSPS



Spectral Response, 120 MSPS



Spectral Response, 180 MSPS



Spectral Response, 216 MSPS

