Ultra Wideband Digital Down Converter – BW of 500 MHz

Rev 1.0

II proposed the following signal processing core for the 500 MHz bandwidth DDC. X6-GSPS is under-sampling the 500 MHz bandwidth signal carried on 1 GHz IF at the rate of 1.3 GHz. The image signal in the first Nyquist zone is tuned at 400 MHz, spectrum inverted, and put through the filter bank to remove out-of-band signal and noise. The 16-bit outputs of the core are stored in the high speed data logger through PCI Express Gen2 interface.

Illustration 1: X6-GSPS for 500 MHz bandwidth DDC receiver

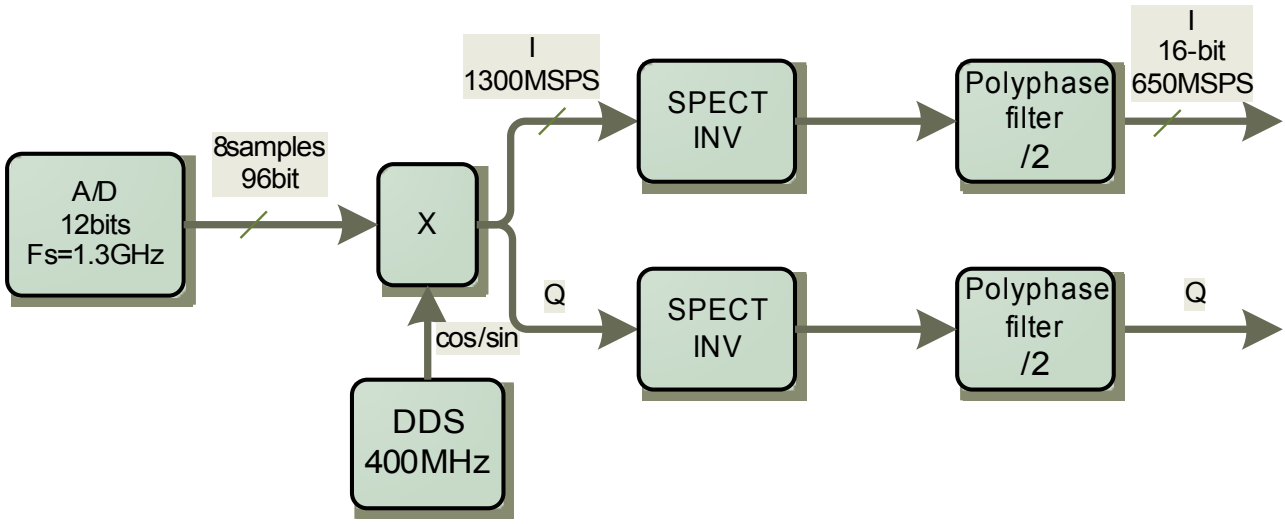

Illustration 2: DDC block diagram for 500 MHz bandwidth of signal

In Illustration 3, the target signal is filtered with the analog bandpass filter to remove out-of-band noise and signal before going to the module. A/D converters perform under-sampling on the input signal and bring it to the first Nyquist zone.

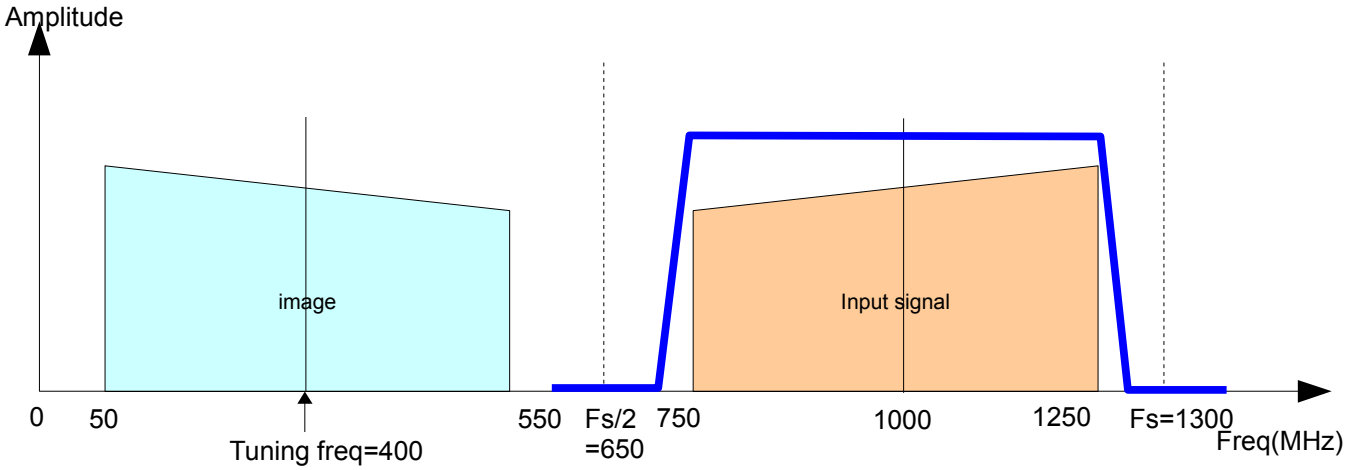

Illustration 3: The location of image after analog bandpass filtering (blue) and under-sampling; where Fs is the A/D sampling frequency.

In Illustration 4, the image above is spectrum inverted and tuned to the base-band with the low-pass filters in the DDC.

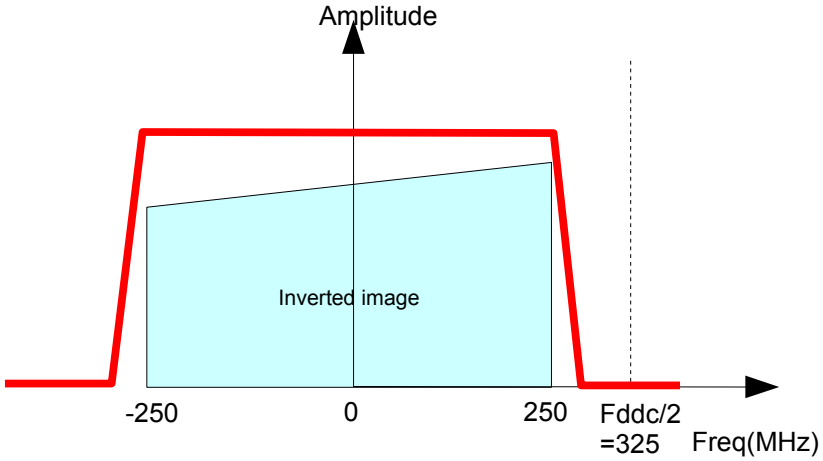

Illustration 4: The baseband signal with the DDC low-pass filtering (red line); where Fddc is the output data rate of DDC.

Specifications

Feature		Specification
500 MHz Bandwidth DDC on X6-GSPSM		
	Digitizing rate	1300 MHz
	Digitizer resolution	12-bit
	Channels	1 (I/Q)
	Channel Tuning	Default to 400 MHz; 0.04 Hz resolution; software programmable.
	Channel Bandwidth	500 MHz, programmable filter coefficients
	Data Transfer Rate	16-bit of I/Q data: 2.6 GByte/s

Table 1: 500 MHz Bandwidth DDC receiver features