Digital Receiver V614

v1.0

PC-based Instrument with Single Ultra Wideband DDC, Spectrum Analyzer and Two XMC Module Sites

System Features

- Intel i7 Quad Core, 16 GB RAM, 240 GB SSD, dual 10 GbE, Win 7 Pro 64-bit
- Two, independent XMC module sites
- Sustained logging rate up-to 2,000 MByte/s

Per- XMC Module Features

- Two 12-bit, 1.8 GHz ADCs
- Analog bandwidth: 1MHz - 2GHz(AC Coupled)
- Xilinx Virtex-6 SX475T-2 FPGA
- Embedded power meter
- PCI Express Gen 2 (3,200 MByte/s)

Digital Down-Converter (DDC)

- Single 8-bit DDC channel
- Programmable tuner: 1 MHz - 1.8 GHz; resolution 0.4191 Hz
- Programmable bandwidth: 60 - 750 MHz
- DDC outputs SNR > 40 dB; SFDR > 60 dB
- Spectrum inversion for ADC under-sampling
- Support synchronous down-sampling on multiple channels and modules using external clock/trigger
- Synchronous VITA-49 timestamp

Spectrum Analyzer

- Single wide-band/narrow-band 32K points FFT
- Eight Windowing available
- Programmable FFT update rate
- Programmable maximum hold mode
- Threshold limited spectrum monitoring up-to 512 bins

Applications

- Digital Receiver
- Spectrum Analysis
- Surveillance
- Software Defined Radio

Description

The V614 digital receiver supports one or two plug-in XMC modules each featuring one ultra-wideband DDC and one spectrum analyzer embedded in the Xilinx Virtex-6 FPGA. It supports monitoring and/or recording of wide- or narrow-band spectra or channelized IF band data. The receiver supports contiguous recording at 2000 MByte/s until running out of disk space.

The DDC has its own programmable tuner, programmable low-pass filtering, gain control, and decimation settings, supporting output bandwidth up-to 750 MHz. Data is packetized in VITA-49 format with accurate timestamps, synchronous to an external PPS signal. Each DDC channel can be enabled and disabled on the fly to conserve host computer storage and bandwidth. An embedded power meter monitors the power (dBFS) of the ADC inputs, supporting analog gain control of optional, user-supplied external front-end devices.

The spectrum analyzer, including windowing, calculates the wide-band spectrum of the ADC data or the narrow-band spectrum of the DDC output data at the programmable update rate. The maximum hold helps to retain the information in the spectrum and the programmable threshold monitoring spectrum detects the spectral activities up-to 512 bins.

A development kit is available to facilitate custom designs. Users can insert custom-made cores within the provided Framework to create more advanced applications, including features such as demodulation, decoding and error correction.

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System Characteristics

System Parameters (See ePC-Duo datasheet for full embedded PC details)		
	Number of XMC Modules Support	1 or 2
	SBC Type	Intel i7 Quad Core, 16 GB RAM, 240 GB SSD, USB3.0 x2/2.0 x2, 1 GbE x2
	Sustained Logging Rate	500 MByte/s; 2000 MByte/s with additional SSD drives
Module Parameters (See X6-GSPS datasheet for full module details)		
	A/D Converter	Two 12-bit, sampling rate from 1.4 - 1.8 GHz; analog bandwidth 2 GHz (AC Coupled)
	FPGA Type	Xilinx Virtex-6 SX475T-2
	VITA-49 Timestamp	Yes
	Digital-IO	32-bit (Optional)
	PCI Express	One x8 Gen 2 per-module, sustained data rate 3,200 MByte/s
	Digital Down-Converter	
	Channel Number	1
	Channel Tuning	Programmable from 1 MHz - 1.8 GHz; default to 321 MHz.
	Channel Bandwidth	Programmable from 60 - 750 MHz; default to 500 MHz.
	Decimation Rate	2, 4, 8
	Spectrum Inversion	Yes
	SNR	> 40 dB
	SFDR	> 60 dB
	Spectrum Analyzer	
	Number of Core	1
	Windowing	Rectangular, Hann, Chebyshev, Taylor, Blackman-Harris, Hamming, Gaussian, and Flat top.
	Update Rate	Programmable
	Maximum Hold	Programmable
	Spectrum Mode	Full spectrum (FS): 32768 points FFT in natural order; Threshold limited spectrum (TLS): Programmable threshold monitoring up-to 512 bins

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System Block Diagram

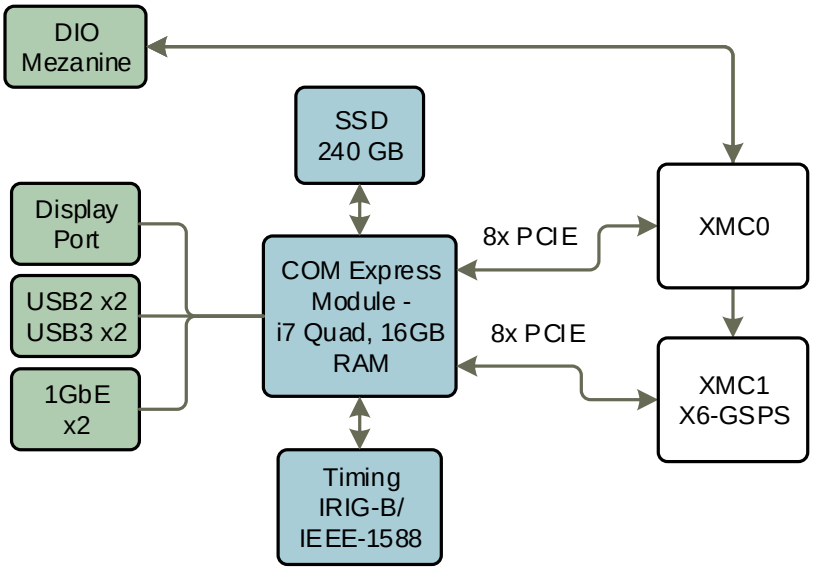

Figure 1. Digital receiver block diagram

Module Block Diagram

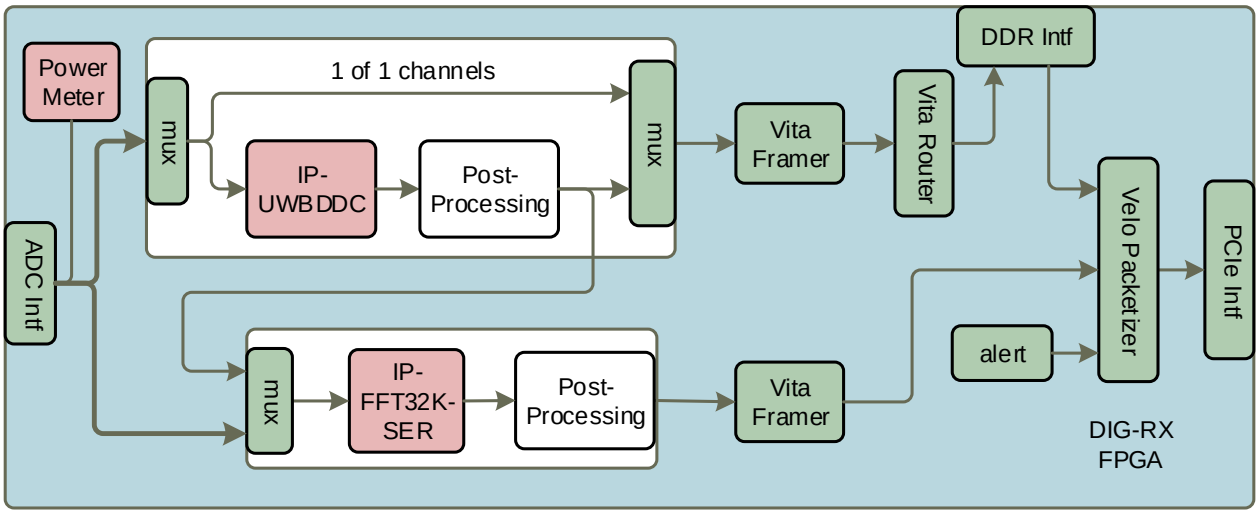

Figure 2. X6-GSPS block diagram

Programmable DDC Filter Characteristics

Fs=1.8 GHz, DDC Bandwidth=750 MHz

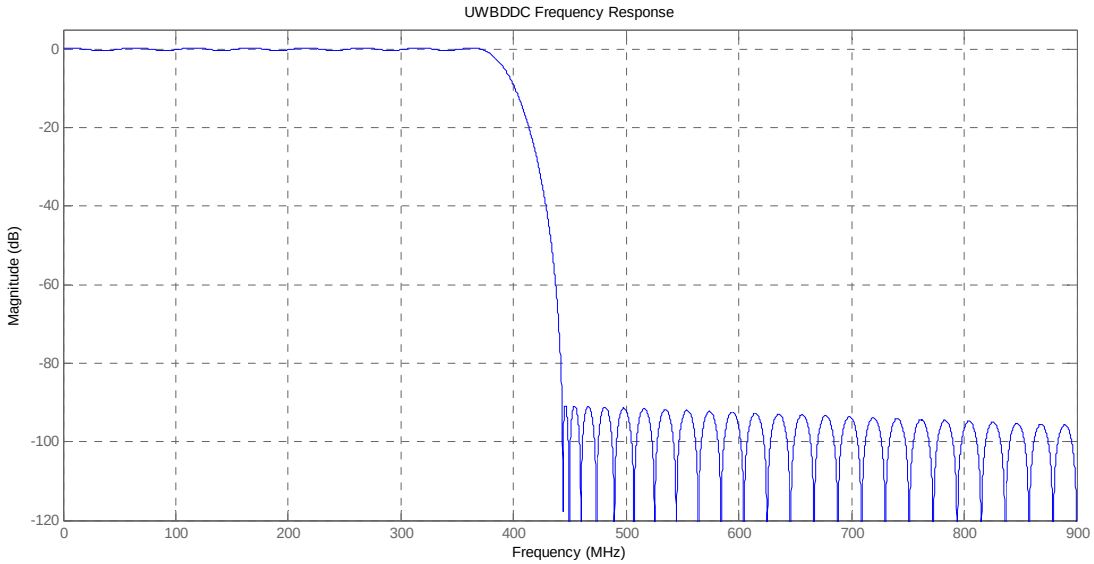

Figure 3. Bandwidth 750 MHz DDC frequency response

Fs=1.8 GHz, DDC Bandwidth=500 MHz

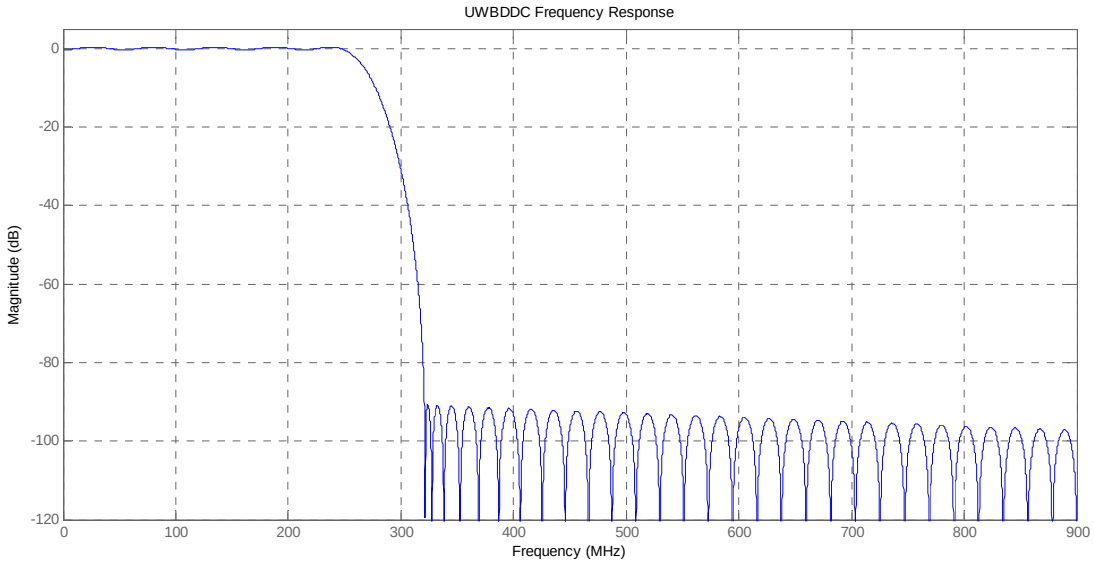

Figure 4. Bandwidth 500 MHz DDC frequency response

Fs=1.8 GHz, DDC Bandwidth=60 MHz

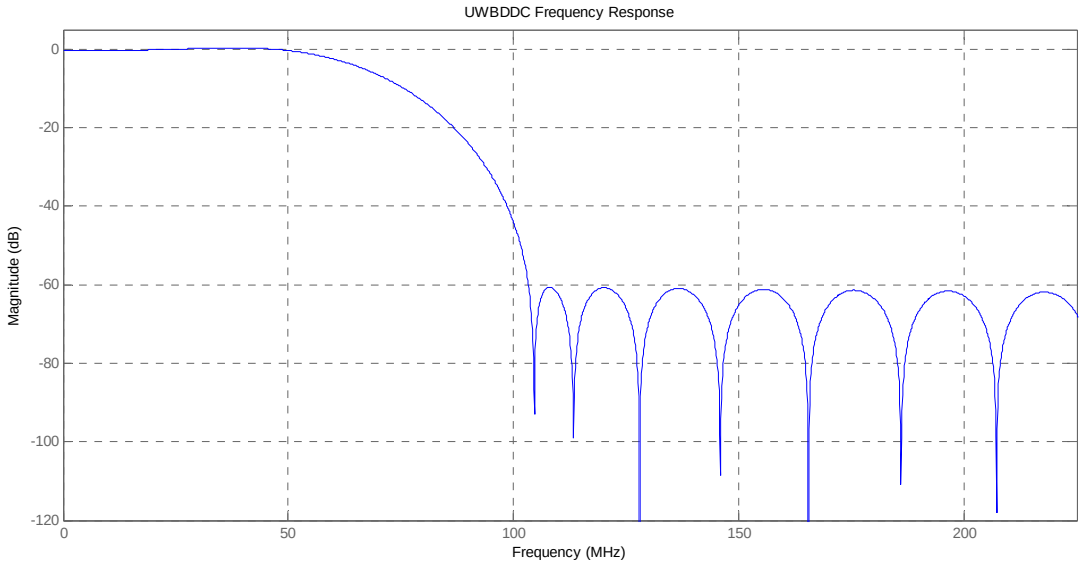

Figure 5. Bandwidth 60 MHz DDC frequency response

Example

Figure 6. **Test environment; anti-aliasing filter is used between the digital receiver and functional generator**

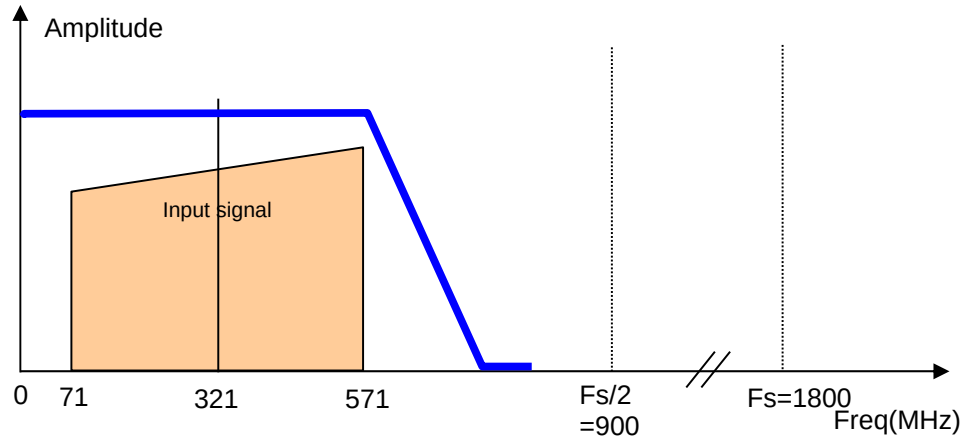

Figure 7. **Bandwidth 500 MHz input signal modulated at 321 MHz; blue line is the shape of anti-aliasing filter; Fs is the ADC sampling frequency.**

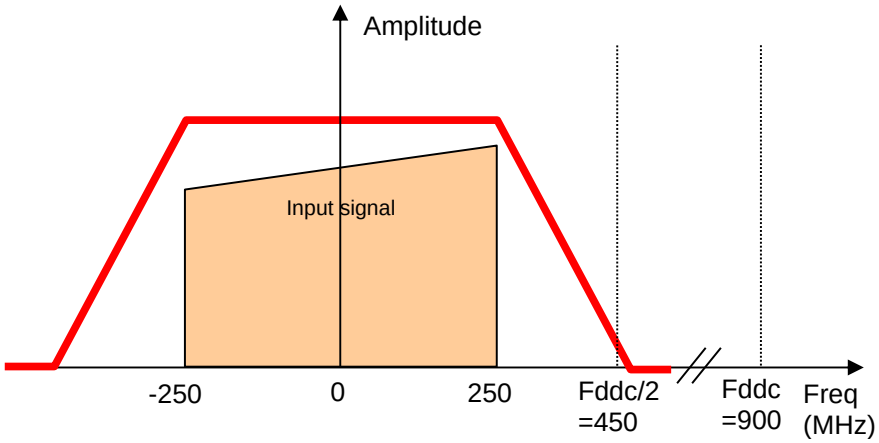

Figure 8. **Down-converted signal to the baseband; red line is the shape of DDC filter; Fddc is the DDC output rate.**

Fs=1.8 GHz, Fin=331 MHz, Ftune=321 MHz, DDC Bandwidth=500 MHz; source: Agilent N5182A, ampl: 4.5 dBm; Lowpass filter: Mini-Circuits SLP-550+

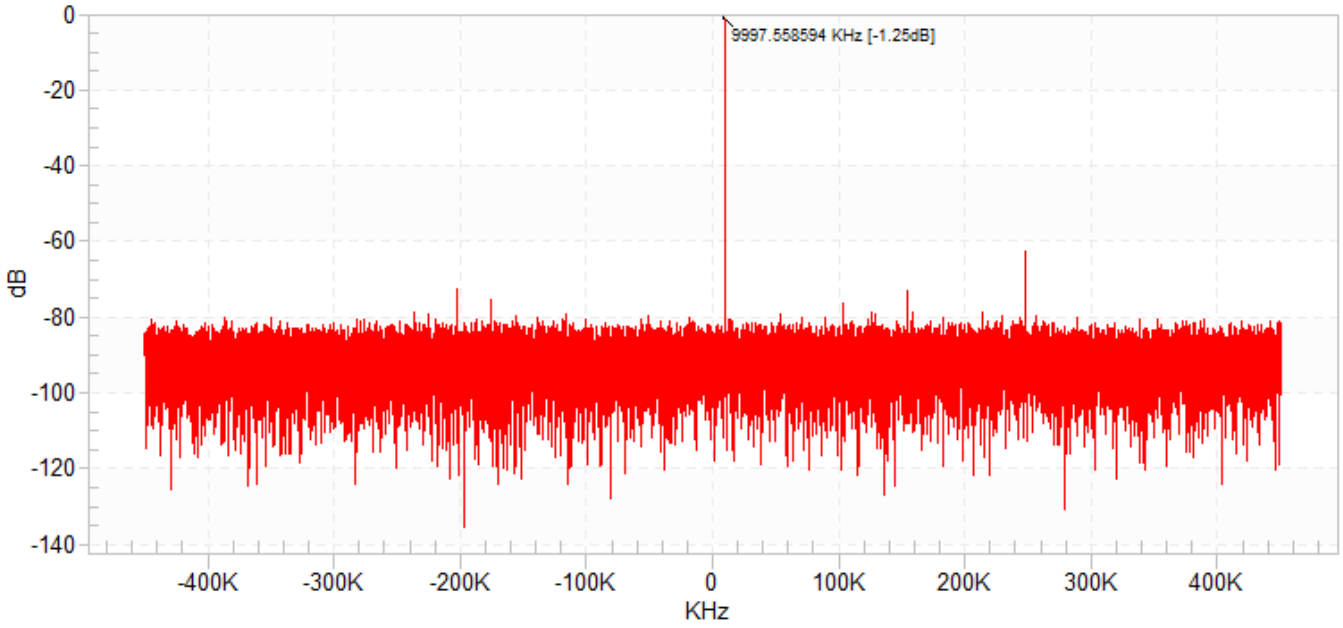

Figure 9. **DDC output complex spectrum in BinView (32768 points FFT); SNR: 42.1 dB, SFDR: 60.9 dB, ENOB: 6.7 bits.**

Software GP-GSPS

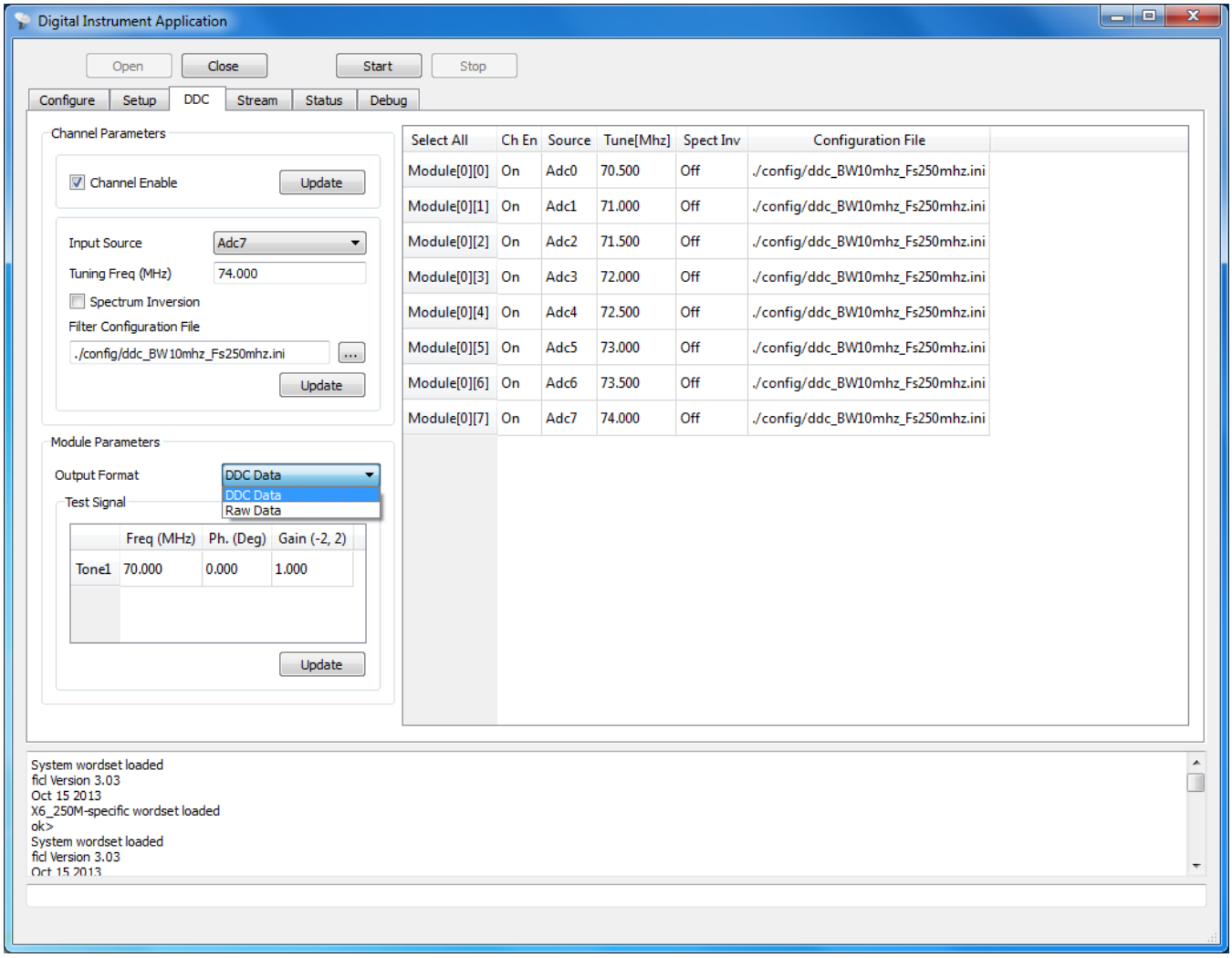

Figure 10. Application software supported in Qt environment

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Ordering Information

Digital Receiver Instrument

Product	Part Number	Description
V614 Digital Receiver Instrument	90616-0-L0	Basic Instrument with single X6-GSPS module, SW/FW PKG, ePC-Duo, 240GB SSD, Win7 Pro 64-Bit
Second X6-GSPS Module	80264-4-L0	X6-GSPS with SX475T2 FPGA, PCIe 8-lane gen1, AC-coupled with SX475T2 FPGA, providing two additional wideband receiver channel driving 2 DDCs and FFT

Development Kit

Product	Part Number	Description
UWBDDC and Spectrum Analysis	55201-1	Framework Logic – 1 channels of IP-UWBDDC and 1 channel of IP-FFT32K-SER for X6-GSPS Virtex-6 SX475T2

Accessories and Hardware

Product	Part Number	Description
Cables		
SMA to BNC Cable	67048	IO cable with SMA (male) to BNC (female), 1 meter
Storage		
SSD 240 GB	36038	Corsair Neutron Series GTX CSSD-N240GBGTXB-BK 2.5” 240GB SATA III
SSD 512 GB	36043	SAMSUNG 840 Pro Series MZ-7PD512BW 2.5" 512GB SATA III

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