

Product Guide | Volume 23



DSP Data Acquisition Embedded Control



### Innovative DSP, Data Acquisition & FPGA Products

Since 1988, Innovative Integration has grown to become one of the world's leading providers of signal processing and data acquisition hardware and software. Our products combine FPGAs utilizing optimized digital signal processing algorithms with high performance analog, ready for integration into demanding real-time applications such as wireless, medical, and military. Our product family includes, PCI Express, XMC, FMC modules, Multichannel Transceiver Systems, Digital Receiver Systems, Data Loggers, Wireless IP Cores, and development support software tool sets specifically engineered for high performance embedded DSP and computing applications.

Customization is in our DNA and is available for any product to help you meet your cost and performance goals in volume applications. Teaming up with our parent company, Interconnect Systems, Inc. - www.isipkg.com, has given us the ability to be your one-stop shop. Our capabilities include manufacturing and packaging of COTS and semi/full custom electronics. Browse this guide, then contact us directly to find out how we can meet your specific needs - our design team is ready to deliver.

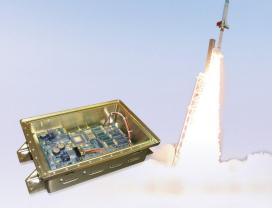
**Jim Henderson** 

Jim Henderso President



# **Real World Solutions**

... for the global market



# Our Innovative Architectures at Work

Innovative Integration boards are integrated in a wide array of applications, at the leading edge of most engineering fields, in one-of-a-kind, esoteric systems as well as large volume OEM equipment. Whatever your challenge, we can assist you.

The applications listed below are actual systems developed by our customers using Innovative Integration DSP, data acquisition and embedded control solutions.



Medical Imaging High-speed MRI and Ultrasound



Wireless Multi-channel Satellite Receiver JTRS Test and Verification Wideband Surveillance Cellular Test



Industrial Control Magnetic Bearing Servo-Control Ultrasound Material Inspection Multi-Axes Motion Control Soil Analysis While Oil-Drilling Seismic Soil Test



### OEM Instruments

Atomic Force Current Tunneling Scanning Microscope Wafer Flatness Measurement Tool Wafer Surface Inspection Station Active Vibration Control Table for Lithography In-situ Optical Measurement for Plasma Etching Active Noise Cancellation



Military Hardware Flight Data Recorder Aircraft Hydraulic Actuator Testing Guidance Controls



Telecom/Intelligence Software Defined Radio using OFDM Technology Joint Tactical Radio System Development Military Radio Test Equipment Digital Receiver Direction Finder Acoustic Direction Finder



SONAR Hydrophone Transient Detection Rocket Engine Control



**Bio-Medical** Cardiac Assist Pump Genetic Slide Generation Bionic Ear Development Atom Interferometry



Research & Development Laser Communication Optics Control Laser Telescope Control Ultra-High Precision Motion Chemical Agent IR Detection

Ring-Down Cavity Spectroscopy



Test & Measurement Jet Engine Vibration Analysis Wireless Chip Semiconductor Test Disk Drive Testing DSL Modem Testing Acoustic Wind Tunnel for Aircraft

Whitepapers and datasheets are available for download at www.innovative-dsp.com

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### Solutions for Advanced Data Acquisition, Signal Processing and Embedded Systems - off the shelf!

Since 1988, Innovative Integration has been delivering a rich mix of Data Acquisition, DSP (Digital Signal Processor) and FPGA (Field Programmable Gate Array) boards with productive support tools, providing off-the-shelf solutions to developers of high-end signal capture and co-processing software.



Kintex-7 FPGAs deliver high signal processing performance and low power consumption at price points required for wireless networks.



Largest State of the Art FPGAs for End-user Code Xilinx Spartan 2/3, Virtex II & Virtex II-Pro, Virtex-5, Virtex-6 (LX and SX)



Analog I/O & High Speed Digital Interfaces Fully integrated on-board, with burst interfaces, up to 3 GHz digitizing speed or >3 GHz and >120 dB dynamic range SNR



Rapid Application Development Matlab & C++ support, drivers, libraries, code examples operating peripherals at full speed

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With strong partnerships with Texas Instruments, Xilinx and The MathWorks, Innovative Integration delivers superior architectures and development tools that allow customers to be first to market in their respective field of expertise.













**£** XILINX.



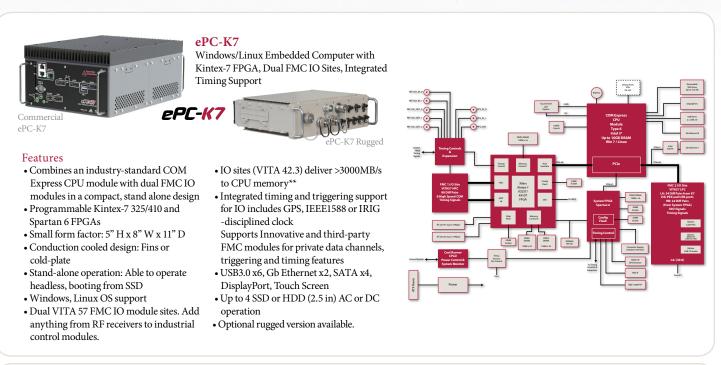
# **Kintex-7 Products**

High signal processing performance Low power consumption **Excellent for Wireless applications** 



### **Kintex-7** Products

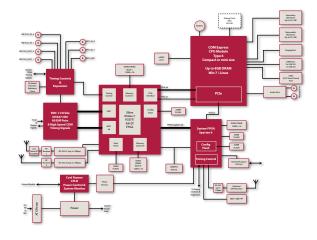
Kintex-7 products deliver high signal processing performance and low power consumption at price points required for the deployment of Long Term Evolution (LTE) wireless networks. These products meet the aggressive power and cost requirements and delivers the serial bandwidth needed for Embedded Instrumentation and Controls, Distributed Sensor Process and Networks and Remote Data Recording.





- Combines an industry-standard COM Express CPU module with a single FMC I/O module in an extremely compact, stand alone design
- Programmable Kintex-7 325/410 and Spartan 6 FPGAs
- Small form factor: 4" H x 7" W x 10" D
- Conduction cooled: Fins or cold-plate • Stand-alone operation: Able to operate
- headless, booting from SSD
- Windows, Linux support. RTOS available. • VITA 57 FMC IO module site. Add anything from RF receivers to industrial control modules.

- IO site (VITA 42.3) delivers >3000MB/s to CPU memory\*\*
- · Integrated timing and triggering support for IO includes GPS, IEEE1588 or IRIG-disciplined clock
- Supports Innovative and third-party FMC modules for private data channels, triggering and timing features
- USB 3.0 x2/2.0 x2, Gb Ethernet, SATA x4, DisplayPort, Touch Screen
- Up to 2 SSD (2.5 in)
- · AC or DC operation







# **FMC Products**

# Wide range of dense, high-performance I/O solutions in VITA57 form-factor

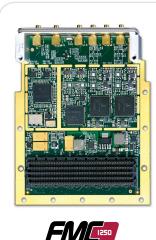
### FMC Products

The FMC standard was created to provide a standard mezzanine card form factor, connectors, and modular interface to an FPGA located on a base board (carrier card). Decoupling the I/O interfaces from the FPGA in this manner simplifies I/O interface module design while maximizing carrier card reuse.

Module	A/D	D/A	Other I/O
FMC-1250	2x 1250 MSPS, 14-bit/16-bit option	2x 1250 MSPS, 16-bit	PLL
FMC-500	2x 500 MSPS, 16-bit	2x 1250 MSPS, 16-bit (1 x 1 GSPS, 16-bit)	PLL
FMC-310	4x 310 MSPS, 16-bit		PLL
FMC-250	2x 250 MSPS, 16-bit	2x 1200 MSPS, 16-bit	PLL
FMC-SFP+			4x SFP+ ports

The FMC standard requires only the core I/O transceiver circuitry that connects directly to the FPGA on the carrier card. The resulting efficiencies translate to substantial benefits.

The FMC modules deliver a wide range of solutions: High Speed Digitizing Signal Generation for Wireless Transceiver Pulse Generation, Medical Imaging, Precision Recording/Playback, RADAR, LTE WiMAX Physical Layer, Wireless Receiver and Transmitter, Remote Radio Head receiver, OBSAI and CPRI interface, Serial FPDP and SRIO fiber optic ports.

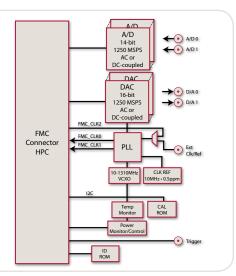


### FMC-1250 FMC Module

Ideal for Wireless Receiver and Transmitter, LTE, WiMAX Physical Layer, RADAR, Medical Imaging, High Speed Data Recording and Playback

### Features

- Two A/D Inputs
- 1250 MSPS, 14-bit
- 1250 MSPS, 16-bit option
- AC or DC coupled
- Two D/A Outputs
  1250 MSPS, 16-bit D/A
- Sample clocks and timing and controls
- FMC module, VITA 57.1
- 6W typical (AC-coupled inputs)
- Conduction Cooling per VITA 20 subset
- Environmental ratings for -40° to 85°C, 9g RMS sine, 0.1g2/Hz random vibration



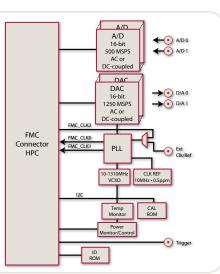




### FMC-500 FMC Module

Ideal for Wireless Receiver and Transmitter, LTE, WiMAX Physical Layer, RADAR, Medical Imaging, High Speed Data Recording and Playback

- Two A/D Inputs
- 500 MSPS, 16-bit
- AC or DC coupled
  Two D/A Outputs
- 1250 MSPS, 16-bit D/A
- Sample clocks and timing and controls
- FMC module, VITA 57.1
- 6W typical (AC-coupled inputs)
- Conduction Cooling per VITA 20 subset
- Environmental ratings for -40° to 85°C, 9g RMS sine, 0.1g2/Hz random vibration



# **FMC Products**



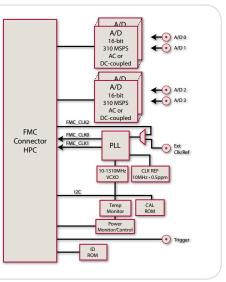
# FMC

### FMC-310 FMC Module

Ideal for Wireless Receiver and Transmitter, LTE, WiMAX Physical Layer, RADAR, Medical Imaging, High Speed Data Recording and Playback

### Features

- Four A/D Inputs
- 310 MSPS, 16-bit
- AC or DC coupled
- Sample clocks and timing and controls - External clock/reference input
- FMC module, VITA 57.1
- 6W typical (AC-coupled inputs)
- Conduction Cooling per VITA 20 subset
- Environmental ratings for -40° to 85°C, 9g RMS sine, 0.1g2/Hz random vibration



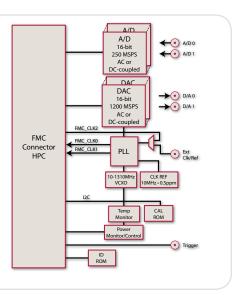


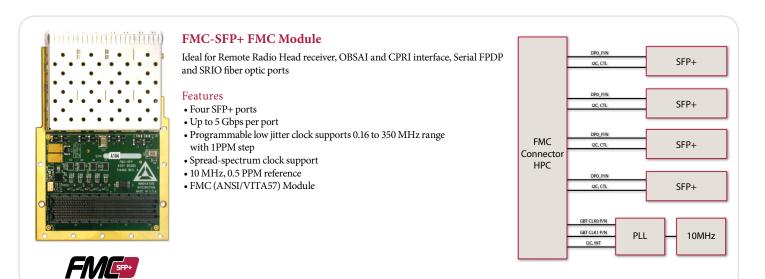
**FM**<sup>250</sup>

### FMC-250 FMC Module

Ideal for High Speed Digitizing, Signal Generation for Wireless Transceiver Pulse Generation, Medical Imaging, Precision Recording/Playback

- Two A/D Inputs
  - 250 MSPS, 16-bit option
  - AC or DC coupled
- Two D/A Outputs
- 1200 MSPS, 16-bit D/A
- AC or DC coupledSample clocks and timing and controls
- External clock/reference input
- FMC module, VITA 57.1
- 6W typical (AC-coupled inputs)
- Conduction Cooling per VITA 20 subset
- Environmental ratings for -40° to 85°C
- 9g RMS sine, 0.1g2/Hz random vibration











### Features

- FMC I/O site (VITA 57) with x10 5 Gbps MGT lanes, 80 LVDS pairs (LA, HA, HB)
- Virtex-6 SX315T/475T, LX240T/550T
- 2 Banks 1GB DRAM (2GB total)
- 2 Banks 9MB QDRII+ SRAM (18MB total)
- 128MB DDR3 DRAM

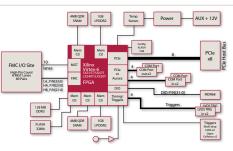
### PEX6-COP

PCI Express Desktop/Server Coprocessor with Virtex6 FPGA computing core and FMC IO site for Wireless Receivers (LTE, WiMAX, SATCOM), RADAR, Signal Intelligence, Medical Imaging, High Speed Data Record/Play, IP Development

- 32Mb FLASH
- Dual sample clock inputs
- High speed trigger inputs support multicard sync & coordinated sampling
- Gen2 x8 PCI Express providing 4 GB/s burst and 2 GB/s sustained transfer rates

• 2 Banks of 9MB QDRII+ SRAM (18MB total)

• Global and local timing and triggering



- x4 Secondary Port usable as PCIe or Aurora
- < 15W typical excluding FMC
- Configures from on-card FLASH
- High temp option: 0 to +85 °C



• 3U OpenVPX FPGA coprocessor card

• FMC I/O site (VITA 57) with 8x 5 Gbps MGT

lanes, 80 LVDS pairs (LA, HA, HB full support)

• Xilinx Virtex-6 SX315T/475T LX240T/550T

• 2 Banks of 1 GB DRAM (2 GB total)

• FPGA Computing Core

### VPX6-COP

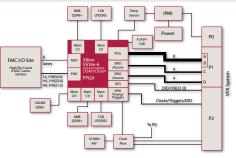
Wireless Receivers (LTE, WiMAX, SATCOM), RADAR, Signal Intelligence, Medical Imaging, High Speed Data Recording and Playback, **IP** Development

• 128MB DDR3 DRAM

Gen2 x8 PCI Express

• 2 GB/s sustained xfer rates

• 4 GB/s burst



- 2 Serial RapidIO or Aurora ports x4 Gen2 (2 GB/s)
- < 15W typical excluding FMC
- Ruggedization Levels up to L4
- Forced air or conduction cooling
- 40g shock 9g sine 0.1 g2/Hz random vibe



ePC-K7

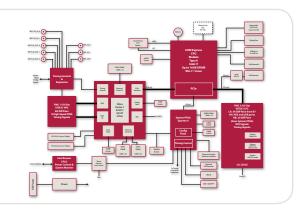
Features

Features • See page 5 for details



Windows/Linux Embedded Computer with Kintex-7 FPGA, Dual FMC IO Sites, Integrated **Timing Support** 



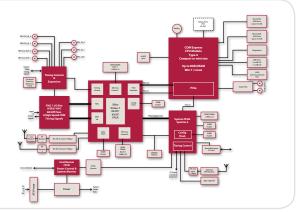




Features · See page 5 for details

### mini-K7

Windows/Linux Embedded Computer with Kintex-7 FPGA, FMC I/O Site, Integrated **Timing Support** 





# **VPX Products**

# Rugged, high-bandwidth products in 3U OpenVPX form-factor



### VPX Products

VPX is an ANSI/VITA standard that provides support for switched fabrics over a new high speed connector. It has been designed specifically with high-reliability and defense applications in mind, with an enhanced module standard that enables applications and platforms with superior performance. VPX is available in 6U and 3U form factor and supports existing PMC and XMC mezzanines.



### Features

- 3U OpenVPX embedded computer system
- Integrated timing and triggering
- Advanced multiple plane connectivity
- Rugged with wide-temperature options
- COM Express module with Intel i5/i7
- 8GB RAM max Windows/Linux/VxWorks
- Gb Ethernet/4x USB/DisplayPort video
- 256GB SSD + up to 3 removable drives
- Half (1/2) rack, 4U system
- 5 slots: CPU 4 OpenVPX Storage/IO
- Supports II X3/5/6 modules & VPX-COP
- Multiple Data Plane Support
- PCI Express and SRIO planes
- Mesh interconnects all IO cards
- Front panel x4 optical link for SRIO IO

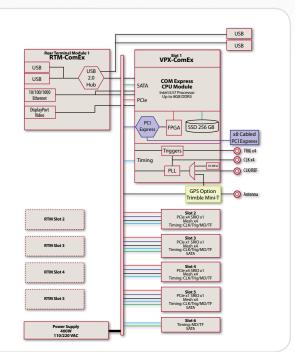
Remote, Autonomous IO, Mobile Instrumentation, Distributed Data Acquisition,

Signal Processing Clusters

VPXI-ePC



- Integrated timing and triggering features
- Synchronized, multi-card sampling
- Internal or external clock/references
- Low phase noise sample clocks (0.125-1GHz)
- 10MHz, 0.5 ppm stable clock reference
- Optional GPS-disciplined reference
- Rear Terminal Modules for I/O, CPU slots
- · Forced air cooling with upper & lower fans
- Integrated 400W power supply
- Expands to additional VPXI chassis using Cable PCI Express option





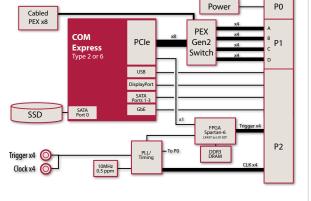
### Features

- 3U OpenVPX VITA65 CPU card
- Runs Windows, Linux, VxWorks
- COM Express Type 6 CPU module
- Intel i7 up to Intel i7 Quad-core CPU
- Up 16GB 1333MHz DDR3 ECC memory
- PCIe Root supports x4/x4/x1/x1 endpoints
- GbE, USB 2.0, 3x SATA 300, DisplayPort
- Integrated 1.8 in SATA SSD up to 256 GB
- PCI Express Switch
- 16 ln to VPX P1 Font panel x8 PCIe cable • Supports system expansion or redundancy
- < 50W typical; conduction or forced-air

### **VPX-ComEx**

VPX System CPU, DSP for RADAR, Communications, Signal Intelligence Applications, Medical Imaging, High Speed Data Recording and Playback, Embedded Instrumentation and Control

- Precision timing/triggering support
  PLL 125KHz to 1GHz tuning range w/
  - -110 dB phase noise @ 10kHz
- 10MHz, 0.28 PPM clock reference
- Reference input support for GPS
- Synchronized triggering outputs
- Xilinx Spartan-6 LX75T-120T FPGA core • PCIe interface
- 128MB memory
- Operating Environment:
- -40 to 85 °C, 0 to 100% RH
- 30g shock, 0.04 g2/Hz random vibe





PX Back

# **VPX Products**



### Features

- Use w/Cabled PCIe & 3U OpenVPX modules
- 5 slots 4 OpenVPX Peripheral IO Slot • Rear Terminal Modules for peripherals
- Half-rack, 4U enclosure
- Forced air cooling w/upper & lower fans
- · Optional high precision GPS option

### **VPXI Expansion Chassis**

Five Slot 3U OpenVPX Expansion Chassis with x8 Cable PCI Express Host Connection

- Integrated 500W power supply
- Performance architecture supports
- multi data planes & timing/triggering · Centralized control IO & data planes
- · Ring topology mesh
- Timing/triggering features



### VPX6 COP

### Features

- 3U OpenVPX FPGA coprocessor card
- FMC I/O site (VITA 57) with 8x 5 Gbps MGT
- lanes, 80 LVDS pairs (LA, HA, HB full support) • FPGA Computing Core
- Xilinx Virtex-6 SX315T/475T LX240T/550T • 2 Banks of 1 GB DRAM (2GB total)
- 2 Banks of 9MB QDRII+ SRAM (18MB total)
- 128MB DDR3 DRAM

Wireless Receivers (LTE, WiMAX, SATCOM),

VPX6-COP

RADAR, Signal Intelligence, Medical Imaging, High Speed Data Recording and Playback, **IP** Development

- Global and local timing and triggering
- Gen2 x8 PCI Express

**RTM-ComEx** 

expansion for VPXI-ePC

- 4 GB/s burst 2 GB/s sustained xfer rates
- 2 Serial RapidIO or Aurora ports- x4 Gen2 (2 GB/s)
- < 15W typical excluding FMC
- Ruggedization Levels up to L4
- · Forced air or conduction cooling

Rear Terminal I/O Module for VPX-COMEX 3U OpenVPX CPU Card for VPXI-ePC

signal processing applications, Embedded Instrumentation & Control, System timing

• 40g shock • 9g sine • 0.1 g2/Hz random vibe



### Features

- Rear panel I/O: USB 2.0 10/100/1000 Ethernet DisplayPort VPXI Timing Port
- Internal I/O (optional rear panel support): 3x USB 2.0 Sample clock and trigger
- VPXI Timing Expansion Port:
- Extends VPXI timing signals to second chassis or custom equipment
- Synchronize multiple chassis sampling
- GPS: Serial port for comm PPS & 10MHz inputs Supports Trimble Mini-T GPS & others



### Features

- Adapt one XMC module to a 3U OpenVPX
- Config mapping for VPX to XMC com ports
- Configurable Dig IO w/VITA 46.9 maps
- System management using IPMI
- Dual SMB buses

XMC Adapter for 3U OpenVPX

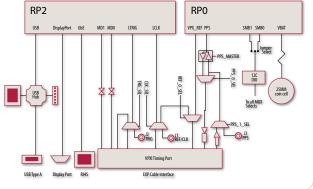
Rugged Conduction or Air Cooled XMC Adapter with IPMI Support

- Power & temperature monitoring
- -40 to +85 °C operation
- 40g shock 0.1 g2/Hz random vibration
- Heat-spreading frame w/direct path to host
- Air Cooling Flow-through air path





XMC

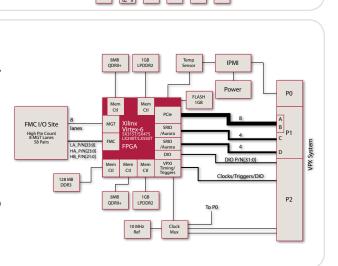


VPX

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P2



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ALL UT

Timing

bal Trigger[1:0]

- VITA20 conduction cooling

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# **Digital Transceiver Instrument**

Precision modular instrumentation

### Digital Transceiver Instrument

Customers at more than 25,000 companies simplify development, increase productivity, and dramatically reduce time to market. Choose your transceiver instrument today and get results for your next Medical, Wide-band Spectral Analysis, or Software Defined Radio applications tomorrow.

### Flexible Instrument

The Digital Transceiver Instrument features eight independent channels of digital down-conversion (DDC) and digital up-conversion (DUC) embedded in Xilinx Virtex-6 FPGA. As a flexible front-end transceiver, this module implements the frequency translation, channelization, and modulation as the FPGA firmware. The Digital Transceiver Instrument is ideal for Wireless Receiver and Transmitter, Spectrum Analysis, Software Defined Radio, LTE, WiMAX Physical Layer, RADAR, Medical Imaging, High Speed Data Recording and Playback, and IP Development applications.

### Features

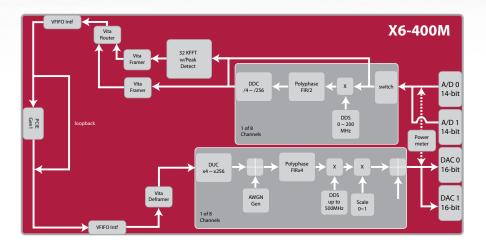
- Two 14-bit analog inputs @ 400 MHz
- Analog input bandwidth: 1 GHz (AC coupled)
- Eight independent 16-bit DDC channels
- DDC max channel bandwidth up-to 50 MHz
- DDC outputs SNR >60 dB; SFDR >76 dB
- Independent tuning from DC ~ 200 MHz; resolution 0.0466 Hz @ 400 MHz sampling rate
- Independent decimation range from 8 to 512
- Programmable CFIR and PFIR (18-bit)
- DDC reprogramming, enable/disable on-the-fly
- Built-in spectrum inversion for under-sampling
- High-speed 32K point parallel FFT with peak detection up-to 512 bins
- Synchronous timestamps with internal 1 sec timer or external PPS signal

### **Transmitter Features**

- One 16-bit analog output @ 1 GHz or two @ 500 GHz
- Analog output bandwidth: 350 MHz(AC coupled)
- Eight independent 16-bit DUC channels
- DUC max channel bandwidth up-to 50 MHz
- Independent tuning from DC ~ 500 MHz; resolution 0.0582 Hz @ 1 GHz sampling rate
- Independent interpolation range from 16 to 1024
- Programmable CFIR and PFIR (18-bit)
- Wide-band AWGN generator.

### **Other Features**

- On-board PLL from 0.3125 ~ 1000 MHz; programmable PFD (default=100 KHz)
- Embedded power meter (-44 dBm ~ 8.5 dBm)
- 32 digital-IO bits





Receiver	90401-1	90401-2	90401-3	90401-4
Analog Bandwidth	250 Mhz	5 Mhz ~ 1 Ghz	5 Mhz ~ 750 Ghz	1Ghz
A/D Resolution	14-bit	14-bit	12-bit	12-bit
Sample Rate	400 Mhz	400 Mhz	1Ghz	1Ghz
DDC Bandwidth Range	120 Mhz ~ 40 Khz			
DDC Channels	4	4	4	4
FFT	optional	optional	optional	optional
Beamforming	optional	optional	optional	optional
Aurora Link	ready	ready	ready	ready
Timestamp	Yes	Yes	Yes	Yes
Transmitter				
Analog Bandwidth	220 Mhz	5 Mhz ~ 350 Mhz	5 Mhz ~ 1 Ghz	600 Mhz
DAC Resolution	16-bit	16-bit	16-bit	16-bit
Sample Rate	1 Ghz /500 Mhz			
DUC Bandwidth Range	120 Mhz ~ 40 Khz			
DUC Channels	4	4	4	4





# **Digital Receiver Instrument**

Precision modular instrumentation

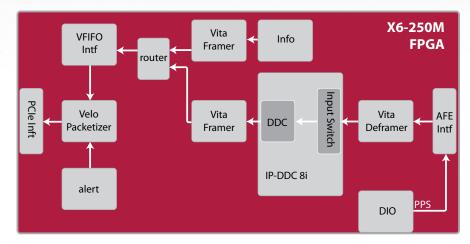
### Digital Receiver Instrument

Innovative Integrations Digital Receiver Instrument boasts speed and accuracy into a new dimension regarding measurements, by utilizing the leading-edge Xilinx FPGA technology. Ultra-fast Analog-to-Digital Conversion as well as real-time signal processing and data playback features offer an ideal turnkey solution for demanding receiver applications such as Spectrum Analysis, Medical Remote Sensing, RADAR, and Software Defined Radio.

### Flexible Instrument

The Digital Receiver Instrument has eight independent output channels of digital down-conversion (DDC) embedded in Xilinx Virtex-6 FPGA. As a flexible front-end receiver, this module implements the frequency translation and channelization for the IF band signal as the FPGA firmware. The Digital Receiver Instrument is ideal for Wireless Receiver and Transmitter, Spectrum Analysis, Software Defined Radio, Wireless Receiver, WLAN, WCDMA, WiMAX front end, RADAR, Medical Imaging, High Speed Data Recording and Playback, and IP Development applications.

- Analog input bandwidth: 400 MHz (AC coupled)
- Eight 14-bit inputs @ max 250 MHz
- On-board PLL from 0.3125 ~ 250 MHz;
- programmable PFD (default=100 KHz)
- Eight independent 16-bit DDC channels
- DDC max channel bandwidth up-to 62.5 MHz
- $\bullet$  DDC outputs SNR >60 dB; SFDR >76 dB
- Independent tuning from DC ~ 125 MHz; resolution 0.0582 Hz @ 250 MHz sampling rate
- Independent decimation range from 4 to 256
- Programmable 20 tap CFIR (18-bit)
- Programmable 80 tap PFIR (18-bit)
- DDC Overflow indicator
- DDC reprogramming, enable/disable on-the-fly
- Built-in spectrum inversion for under-sampling
- Synchronous timestamps with internal 1 sec timer or external PPS signal
- Embedded power meter (-44 dBm ~ 8 dBm)
- 32 digital-IO bits





Receiver	90400-1	90400-2	90400-3	90400-4
Analog Bandwidth	5 Mhz ~ 400 Mhz	500 Mhz	5 Mhz ~ 2 Ghz	5 Mhz ~ 2 Ghz
A/D Resolution	14-bit	14-bit	12-bit	12-bit
Sample Rate	250 MHz	250 Mhz	1.8 Ghz	1.3 Ghz
DDC Bandwidth Range	50 Mhz ~ 200 Khz	50 Mhz ~ 200 Khz	120 Mhz ~ 40 Khz	500 Mhz ~ 32 Khz
DDC Channels	8	8	8	8
FFT	optional	optional	optional	optional
Beamforming	optional	optional	optional	optional
Aurora Link	included	included	included	included
Timestamp	Yes	Yes	Yes	Yes





# elnstruments

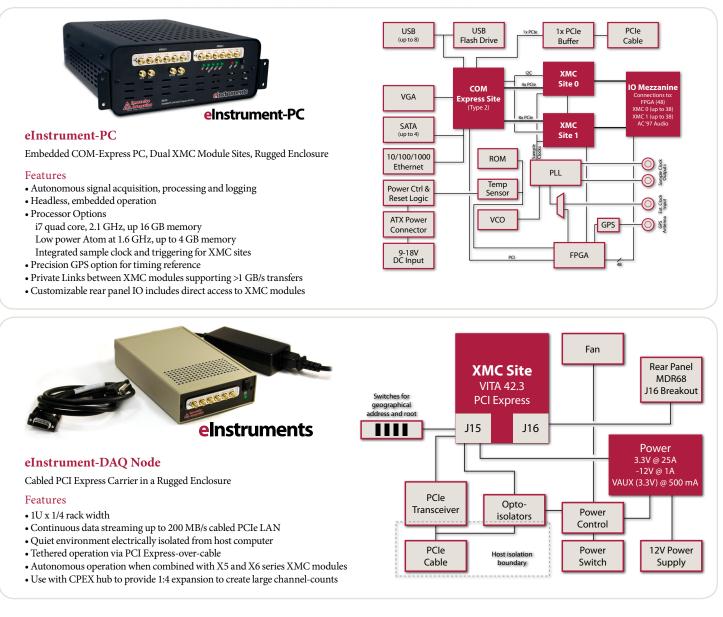
Intelligent Embedded Instrumentation Windows & Linux Compatible Rugged Enclosures

### eInstrument-PC

Miniature Window/Linux embedded PC for standalone or distributed instrumentation using ultimate-performance XMC IO modules. Runs all standard Windows/Linux soft ware just like desktop PC. Intel Penryn i7 Dual core at 2.53 GHz or low power Celeron 1.06 GHz, Up to 4 GB memory, Boot from solid state or hard disk drive. Data logging option: record 1600 MB/s sustained up to 2TB.

### eInstrument-DAQ Node

A large variety of ultimate-performance XMC modules housed in a rugged enclosure featuring an ultra-fast Cabled-PCIe carrier. Position data acquisition near the unit-under-test without sacrificing high-speed connectivity to a Host PC. Software transparent, full electrical isolation for XMC module. PCI Express 2.5 Gbps (~ 200 MB/s).





### Overview

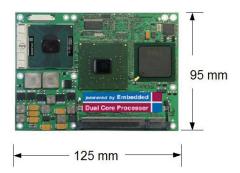
The wireless marketplace is like our nascent universe. A veritable "big-bang" of new radio frequency (RF) technologies have emerged creating opportunities for solving old problems in innovative, new ways. Flexible highresolution waveform generation, digitization and analysis subsystems capable of manipulating RF signals in conjunction with downconversion and tuning multiple "regions of interest" are required. Subsequent, real-time, multi-channel demodulation of these regions using a wide variety of schemes is necessary. Often, such equipment must be portable and operate under harsh environmental conditions creating tremendous challenges in packaging, power consumption and management.

Existing solutions employ arrays of dedicated digital signal processors (DSPs) working in tandem with an RF digitizer to provide the computational bandwidth needed to implement down-conversion and demodulation functions. Though effective, this approach is complicated and expensive since multi-processor programming requires sophisticated process management and load balancing while avoiding race conditions and data bottlenecks. New solutions are emerging as highly-modular devices which leverage the industry-standard, commercial-off-the-shelf (COTS) COM-EX-PRESS PC architecture and development tools in conjunction with PCI Express-based XMC mezzanine modules to create cost-effective, customizable RF processing block solutions.

### Approach

The performance of mainstream DSP devices has effectively stagnated. The system clock on such devices is currently limited to 1 GHz or less, with bandwidth limited to approximately 800 MB/s throughput from the common 100 MHz, 64-bit external bus. By contrast, the x86 architecture continues to evolve, adding instruction set optimizations, enhanced caches, floating point co-processing and multiple cores-on-a-chip with no abatement in sight. Octal core processors featuring 3 GHz processing cores and 10 GB/s external bus bandwidth are ubiquitous. Moreover, the superb Intel Performance Primitives support native signal processing on a x86 processor an order of magnitude faster than existing DSP devices with the added convenience and accuracy of 80-bit floating-point capabilities. However, a desktop or industrial PC does not meet the portability, packaging or environmental requirements of many embedded applications.

Fortunately, due to the immense popularity of the PC as a development and processing tool, the market has already responded with several small-form-factor PC standards which are well suited to creation of embedded, portable instrumentation such as COM-EXPRESS. The COM-EXPRESS format has become a de-facto standard amongst users requiring utmost reliability, scalability, portability and computational performance.



COM-EXPRESS: A rugged PC embedded on a small circuit board

COM-EXPRESS modules are commodity items available from a number of reputable electronics vendors. Pricing ranges from approximately \$300 to \$1300/unit in unit quantities. Pricing is primarily a function of computational capabilities and the required temperature, shock and environmental capabilities required.

COM-EXPRESS modules are small mezzanine modules which are mounted onto a carrier board which is customized to meet specific application requirements.

Innovative Integration has eInstrument-PC to meet the stringent requirements of the embedded RF processing marketplace. Packaged into the companies new eInstrument product, a COM-EXPRESS module, I/O expansion modules and an array of integrated peripherals combine to create a small form-factor, rugged PC which can be embedded within OEM equipment to create intelligent, autonomous instrumentation, servo control or RF processing nodes.

Any mix of the standard peripherals typically found on a PC can be made available in an eInstrument-based system, including Ethernet communications, disk drives, USB and SATA ports. Keyboard and video ports can be provided to aid in field diagnostics. For instance, it is entirely feasible that an eInstrument assembly located in a remote site in a foreign country could be accessed via the Internet using Remote Desktop or VNC by tech support staff at the corporate offices to provide interactive support or software upgrades.

While the cost and computation advantages of a COM-EXPRESS PC compared to traditional chip-level DSP solutions are enormous, a critical side-benefit of the COM-EXPRESS architecture is the ability to leverage the existing body of excellent development and debugging tools available for the PC. Whereas Texas Instruments or Analog Devices are sole sources for compiler and debugger tools for their DSP devices, the PC marketplace sports thousands of well-established providers offering sophisticated, useful, mature tools featuring superior performance and reduced cost. Moreover, conventional desktop PCs may be used to host such tools further accelerating and simplifying the development of COM-EXPRESS-based products.

Though powerful computationally, a COM-EXPRESS PC does not provide direct support for acquisition or analysis of RF analog signals. Moreover, the multi-core x86 CPUs available now and in the foreseeable future do not offer sufficient bandwidth to process RF signals in real-time. Consequently, some form of I/O and processing expansion is required.

Just as COM-EXPRESS provides a PC repackaged into a mezzanine card format, I/O cards are available in a small, rugged form-factor ideal for use in embedded instrumentation. This format is known as PMC (PCI Mezzanine Card). PMC modules support PCI or PCIe (PCI Express) bus communications, identical to that used in standard desktop PCs, but packaged in a small, rugged format.



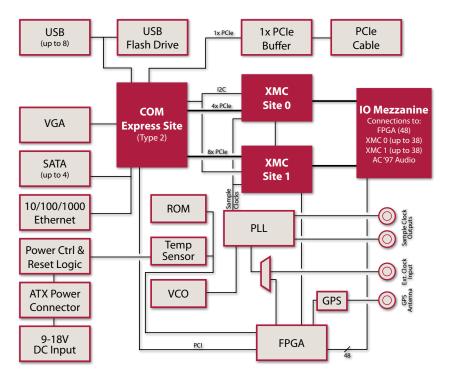
Innovative X6-250M PCI Express PMC module with RF digitizing front-end

PCI Express, the successor to the ubiquitous PCI bus, is the ratified standard replacement for I/O expansion in the PC industry. PCIe features software compatibility with dramatically enhanced throughput up to sixty-four times faster than PCI. Additionally, the bus features guaranteed QoS (quality-of-service) and P2P (point-to-point) data flow capabilities, making it an excellent choice for real-time applications.

The eInstrument COM-EXPRESS PC performs initialization, supervisory control, userinterface as well as high-performance computational duties in RF processing applications. PCI Express-based PMC modules provide I/O and digital signal processing expansion, as illustrated in the block diagram on page 15.



# elnstruments



Block Diagram of Innovative Integration's COM-EXPRESS-based eInstrument carrier card

User interface devices, such as the keyboard, mouse and display may be exposed as diagnostic ports or omitted entirely. Alternately, access to popular embedded user interface controls such as buttons, graphical OLED displays, etc which are commonplace in embedded instrumentation can be provided. Similarly, the USB and hard disk interfaces may be hidden, omitted in the initial design or presented as optional devices available only on designated systems.

eInstruments-based PCs run standard Windows or Linux variants such as XP, Windows 7 or OpenSuse to fully utilize drivers available for existing PMC modules. These PCs are provided with C++ libraries which exploit high performance signal processing features provided in the optimized Intel Performance Primitives library yielding world-class DSP functionality and performance running on an standard x86 platform.

Two PCI Express XMC module sites are provided for I/O expansion. One is typically used to host the a PMC module which implements the RF front-end analog input and output and FP-GA-based digital signal processing capabilities. The second site is uncommitted and available for future expansion. A bevy of PCIe-compliant PMC modules compatible with these sites are available to provide additional capabilities such as fiberchannel ethernet communications, auxiliary voice or ultrasonic-band analog channels or additional FPGA resources. Each eInstrument site features four or eight 2.5 Gbps PCI Express I/O lanes which is essential to support sustained high speed data transfers. Sustained module-host transfers at 1 GB/s are readily achievable, even under non-real-time operating systems such as Windows XP or Linux. Additionally, the two sites provide eight dedicated communications lanes to allow implementation of algorithms in which large volumes of data are shared between modules. Even accounting for lane inefficiencies, sustained intersite data rates of 1.8 GB/s are realized.



The eInstrument embedded PC with modular DSP packaged into an  $7^{\circ} \times 10^{\circ} \times 3^{\circ}$  chassis.

The PCI Express bus provides excellent, highbandwidth connectivity between the COM-EX-PRESS CPU and the PMC module. Given the 1 GB/s sustained throughput, the interface has sufficient bandwidth for low-bandwidth downconverted baseband data plus plenty of additional bandwidth in reserve should it become desirable to capture or log raw IF data in future applications. PCIe also supports fast random, asynchronous I/O accesses to peripheral registers on XMC modules, to accommodate operations such as filter coefficient uploads, DDC channel tuning, and the myriad other operations typically required in software radio applications. Typical, individual slave-type accesses will complete in under 1 uS using a modern COM-EXPRESS module.

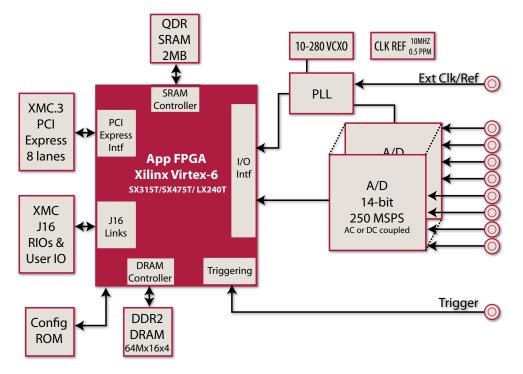
Innovative's new X6 module product family combines the most powerful FPGA ever offered by Xilinx – the Virtex-6, with a variety of RF-speed, high-resolution analog I/O devices, packaged as industry-standard PMC/XMC modules. These products combine up 4 channels of high-resolution analog input and/or output plus an FPGAbased signal processing core that is capable of performing the real-time signal digitizing, data buffering and signal processing required for RF processing applications.

These XMC modules support conduction-cooled operation in accordance with the VITA 20 mechanical specification. Additionally, the standard logic includes provisions for continuous temperature monitoring. Software may receive alerts messages whenever the temperature exceeds a programmed warning threshold temperature and the logic is configured to automatically shut down if the temperature exceeds a programmed failure threshold temperature. This combination of advanced thermal management insures excellent real-world, in-field reliability.

Custom firmware for the FPGA, may be built using standard IP cores and fully modeled under MATLAB, which facilitates high performance and accelerated time-to-market for embedded applications. Custom firmware for the Virtex-5 FPGA builds on the FrameWork Logic, provided by the vendor, to interact with the on-board analog devices, DDR and QDR memory pools and PCI Express bus interface. The firmware works with in conjunction with PC-based software tools and C++ libraries, providing a comprehensive software development system for integration of the PMC with the host application. Data sheets for the Framework Logic and Malibu software libraries may be viewed at http://www.innovativedsp.com/products/software.htm.

In order to provide optimal AC performance, the high-speed RF analog input circuitry must be driven using a stable, low-jitter sample clock. The onboard clock circuit is a derivative of our X3-Timing module product which exhibits < 100 fempto-seconds RMS jitter for 6.25 to 1000 MHz clock range, long-term thermal stability and integrated clock drivers capable of simultaneously sourcing into 50 ohm loads on each of the XMC sites and external devices through the EXT CLK connector.





### X6-250M Block Diagram

In some applications it is desirable to synchronize the module sample clock with world time as provided by a GPS circuit. To accommodate these requirements, the eInstrument carrier features an integrated GPS receiver and sample clock timebase circuitry. Control logic embedded into the carrier FPGA servo-locks to the epoch (1 pps) output events produced by the GPS receiver, insuring that eInstrument PCs located in disparate locations across the world start acquisition and sample synchronously to within 1 uS.

### Embedded Signal Processing

X6 PMC modules are engineered to support RF signal processing applications with minimal external circuitry and with no modification of the X6 bus interface or PCIe back-end infrastructure. For instance, the diagram above shows the X6-250M functional block diagram.

Significant features of the X6-250M module are its high performance analog front end with 4 channels of 310 MSPS, 14-bit A/D, a high performance processing core built around the state-ofthe-art Xilinx Virtex-5 Pro FPGA and memory, sample rate clocking and synchronization, and a high performance packet-protocol PCI Express interface for system integration.

As with all X6 modules, the personality of the 250M FPGA is user programmable using either HDL or MATLAB using Xilinx System Generator. Typically, the FPGA is modified to implement independent down-conversion channels, filters, FFTs and other operations which much be performed at IF frequencies within the FPGA

to forms the basis for baseline RF tuning functionality. The eInstrument COM-EXPRESS PC performs initialization, supervisory control, userinterface as well as high-performance computational duties in such RF processing applications.

The MATLAB board support package for the X6-250M allows signal processing to be developed using MATLAB/SimuLink. SimuLink is used to model the signal processing for bit-true, cycletrue design, which may then be directly tested using hardware-in-the-loop features for hardware testing. This allows the signal processing to be developed at a high level, using proven Xilinx IP cores, and tested in the MATLAB environment.

This technique reduces risk and shortens development time by allowing efficient and thorough verification of the signal processing from within the powerful MATLAB/SimuLink environment. The signal processing logic core from MATLAB is then integrated into the FrameWork HDL for the final logic design.

The Framework Logic package provided with the module provides the hardware interface and support functions such as the A/D interface, memory controllers, host data interface and controls. All standard logic features such as A/D interface, triggering, multi-queue data buffering, DDC control and PCI controller interface are provided as components which must be augmented with custom logic blocks usable in either SimuLink or Xilinx ISE, to form the foundation for the user application firmware.

Ordinarily, the basis for the desired, applicationspecific signal processing functions can be provided by the module manufacturer or from engineering firms specializing in development of such IP, such as RF Engines, Inc. Such firmware may implement customizable digital down-converters, optimized, high-resolution FFT processing blocks capable of operating at a sustained rate in excess of 100 MHz or other capabilities dictated by the application. This is delivered within an extensive training session in which the developed technology is transferred to the client engineering staff. This is the most cost and time-effective development process. Armed with this infrastructure, engineering teams "hit the ground running" and have little trouble modifying the exiting code to meet application-specific requirements.

### Summary

New, ultra-small form-factor PCs allow the creation of a new breed of embedded instrumentation using COTS hardware to lower system cost and improved availability. COM-EXPRESS processor modules provide scalability in host processing power for current and future products. Use of advanced PCI Express PMC modules allows integration of very high-performance FP-GA-based computational engines which can be dynamically loaded with customized firmware to address changing RF processing requirements and markets.

O Brave New World, that has such instruments in it!





# **Andale Data Loggers**

# Turnkey, High-Speed Data Acquisition Up to 48 TB Hard Disk Array

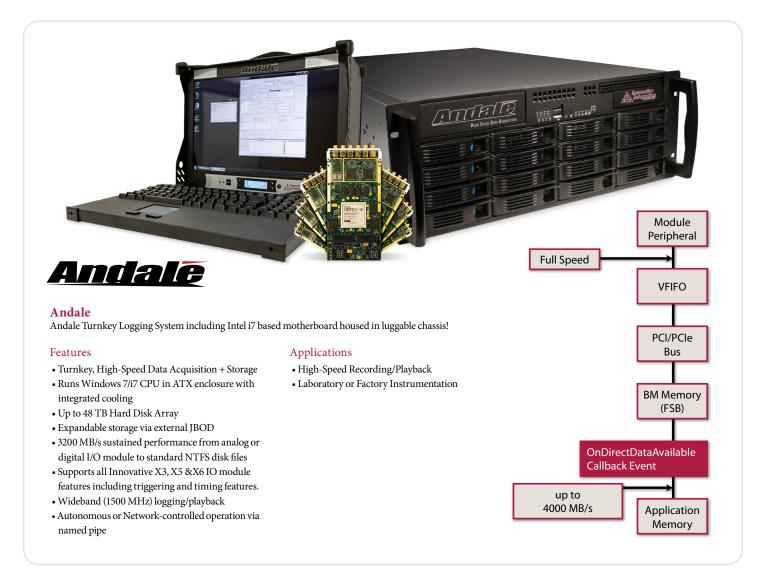
### High Performance, Turnkey Data Logging

Andale (pronounced on' duh lay) is a powerful data logging system which directly controls an NTFS disk subsystem to support gap-free storage or playback of analog or digital signals acquired using the Innovative X-series XMC modules. The included logging software moves data in real-time between the analog or digital I/O peripherals on any Innovative XMC module to/from dedicated SATA drives with minimal intervention from application software or Windows.

Dedicated PCI Express SATA3 RAID controllers interface to conventional hard/SSD drives supporting data flow rates up to 4000 MB/s, sustained. File

sizes are limited only by the amount of disk storage available. Two terabytes of storage are available in the standard configuration; An optional 48 TB configuration is available and even larger storage is supported via external JBOD enclosures. Call Innovative for details.

A multitude of analog/digital I/O interfaces are available through optional XMC modules. Up to four X-series modules with adapters may be installed and operated simultaneously in the chassis.





Intelligent, Customizable I/O High Performance IO and FPGA Core



### High Performance

The X3, X5 and X6 module families feature high performance analog and digital IO on a standard XMC module format with a flexible PCI Express host interface bus. Each has a powerful user-programmable FPGA computing core that is used for data acquisition and connects the I/O to the PCI Express host interface.

### Three Product Groups

The X6 group provides a state-of-the-art combination of the newest generation, high-density, user-reprogrammable Virtex-6 FPGA logic meticulously integrated with ultra-high-speed analog or digital I/O to address the most demanding radar, wireless RF and communications applications.

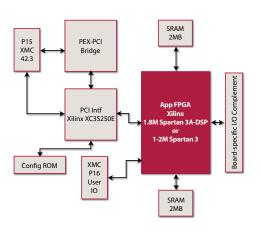
The X3 group provides an extremely cost-effective combination of analog or digital I/O plus a Xilinx Spartan 3 or 3A DSP user-reprogrammable FPGA which provides a plug-and-play, yet customizable solution for common data acquisition, waveform generation and servo/control applications.

The X5 group provides a high-density, user-reprogrammable Virtex-5 FPGA with a PCI Express Gen 1 interface.

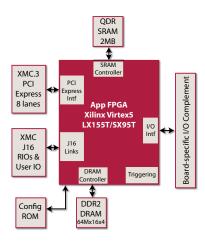
All 3 product groups are usable in a wide variety of hardware platforms. These extremely versatile modules are easily adapted for use in virtually any type of system, Desktop PC, Industrial Chassis, PXI & PXIe Chassis and single board computer based systems. Innovative Integration adapters include CompactPCI, VPX, Desktop PCI & cabled PCI Express systems.

Module	FPGA	Xfer Rate	A/D	Memory	A/D Rate	A/D Res	D/A	D/A Rate	Sample Clock	D/A Res	Digital I/O	Rocket I/O	Special Feature
X6-RX	Virtex-6 SX315T /	2.6 GB/s	4	4 GB	160 MSPS	16-bit	0		PLL or external		64	8	GC6016 DDC
	SX475T or LX240T			(4 banks X 1GB)									24 Channel
X6-400M	Virtex-6 SX315T /	2.6 GB/s	2	4 GB	400 MSPS or	14-bit	2	2 X 500msps	PLL or external	16-bit	64	8	DDC cores for up to 1024 channels available
	SX475T or LX240T			(4 banks X 1GB)	500 MSPS	12-bit	1	1 x 1GSPS					OFDM receiver and transmit IP cores
X6-GSPS	Virtex-6 SX315T /	2.6 GB/s	2	4 GB	2ch.@1.8GSPS	12-bit	0		PLL or external		64	8	Programmable DDC cores available for
	SX475T or LX240T			(4 banks X 1GB)	1ch.@3.6GSPS								wideband channels
X6-1000M	Virtex-6 SX315T /	2.6 GB/s	2	4 GB	1 GSPS	12-bit	2	4 X 500msps	PLL or external	16-bit	64	8	DDC cores for up to 1024 channels
	SX475T or LX240T			(4 banks X 1GB)				2 x 1GSPS					available
X6-250M	Virtex-6 SX315T /	2.6 GB/s	8	4 GB	310 MSPS	14-bit	0		PLL or external		64	8	Very high input channel count
	SX475T or LX240T			(4 banks X 1GB)									
X5-400M	Virtex 5 SX95T	1.3 GB/s	2	512MB DRAM	400 MSPS	14-bit	2	2 X 500msps	400 MHz or	16-bit	38	8	DDC cores for up to 1024 channels
				8 MB SRAM			or 1	1 x 1GSPS	external				available
X5-210M	Virtex 5 SX95T	1.3 GB/s	4	512MB DRAM	250 MSPS	14-bit	0		250 MHz or		16	8	Multi-channel SDR receiver with PSK
				8 MB SRAM					external				demodulator available
X5-TX	Virtex 5 SX95T	1.3 GB/s	0	512MB DRAM			2		PLL or external	16-bit	16	8	Memory controller supports arbitrary and
				8 MB SRAM			or 4						complex pattern playback at full 1 GHz rates
X5-GSPS	Virtex 5 SX95T	1.3 GB/s	2	512MB DRAM	3 or 1.5 GSPS	8-bit	0		PLL or external		16	8	Double rate sampling at 3 GSPS for a single
				8 MB SRAM									channel.
X5-G12	Virtex 5 SX95T	1.3 GB/s	2	512MB DRAM	1 GSPS	12-bit	0		PLL or external		16	8	Double rate sampling at 2 GSPS for a single
				8 MB SRAM									channel, 8K to 256K FFTs in hardware
X5-RX	Virtex 5 SX95T	1.3 GB/s	4	512MB DRAM	200 MSPS	16-bit	0		PLL or external		16	8	Integrated DDC cores for IF processing
				8 MB SRAM									
X5-COM	Virtex 5 SX95T	1.3 GB/s	0	512MB DRAM			0		Prog. oscillator		16	8	4 front panel SFP ports at 3.125 Gbps
				8 MB SRAM					or external				using fiber or copper
X3-2M	Spartan3A DSP -1.8M	220 MB/s	12	4MB SRAM	10 MSPS	16-bit	0		PLL, external		44	0	
X3-10M	Spartan3A DSP -1.8M	180 MB/s	8	4MB SRAM	25 MSPS	16-bit	0		PLL, external		44	0	Simultaneous sampling, pre-triggering mode
X3-25M	Spartan3A DSP -1.8M	180 MB/s	2	4MB SRAM	105 MSPS	16-bit	2	50 MSPS	PLL, external		44	0	Noise floor <95 dB
X3-Servo	Spartan3A DSP -1.8M	180 MB/s	12	4MB SRAM	250 ksps	16-bit	12	1 MSPS	PLL, external	16-bit	44	0	Low latency for servo controls
X3-SDF	Spartan3 -1/2M	180 MB/s	4	4MB SRAM	20 MSPS	24-bit	0		PLL, external	16-bit	44	0	-130 dB noise floor, programmable filters
X3-SD	Spartan3 -1/2M	180 MB/s	16	4MB SRAM	216 ksps	24-bit	0		PLL, external		44	0	>120 dB dynamic range
X3-SD16	Spartan3A DSP -3.4M	180 MB/s	16	4MB SRAM	144 ksps	24-bit	16	144 ksps	PLL, external	24-bit	44	0	>120 dB dynamic range
X3-A4D4	Spartan3A DSP -1.8M	180 MB/s	4	4MB SRAM	4 MSPS	16-bit	4	50 MSPS	PLL, external	16-bit	64 Frnt Pnl LVDS/		Low latency for servo controls
X3-DIO	Spartan3A DSP -1.8M	400 MB/s	0	4MB SRAM			0				LVCM0S44	0	Digital capture, test pattern generation
X3-Timing		180 MB/s	0	0			0		100k to 1GHz		28		Precision sample clock generation with GPS
									sample clock				option

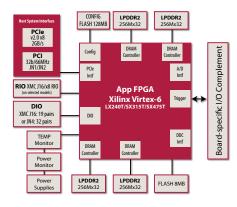




X3 PCI Express XMC Module



X5 PCI Express XMC Module



X6 PCI Express XMC Module

### XILINX® VIRTEX®-6 AC6VSX315T<sup>TM</sup> EFG1156AGW1105 D04209207A

### The X6 Product Group

The X6 Module family has a Virtex-6 FPGA and memory at its core for DSP and control. The Virtex-6 FPGA is capable of

over 1 Tera MACs (SX315T operating at 500 MHz internally) with over 1300 DSP elements in the SX315T FPGA. In addition to the raw processing power, the FPGA fabric integrates logic, memory and connectivity features that make the FPGA capable of applying this processing power to virtually any algorithm and sustaining performance in real-time. The FPGA has direct access to four banks of 1GB DRAM. These memories allow the FPGA working space for computation, required by DSP functions like FFTs, and bulk data storage needed for system data buffering and algorithms like image processing. A multiple-queue controller component in the FPGA implements multiple data buffers in the DRAM that is used for system data buffering and algorithm support.

The X6 module family uses the Virtex-6 FPGA as a system-on-chip to integrate all the features for highest performance. As such, all IO, memory and host interfaces connect directly to the FPGA – providing direct connection to the data and control for maximum flexibility and performance. Firmware for the FPGA completely defines the data flow, signal processing, controls and host interfaces, allowing complete customization of the X6 module functionality. Logic utilization is typically <20% of the device.

X6 products utilize powerful VITA 49 subpackets contained within Innovative's unique Velocia packets, providing up to 3 GB/s data streaming to the host. The payload is flexible and extensible for all types of applications. You can freely mix high rate data streams with control, time-stamps and status making it easy to flow data of different types and rates between the host and the FPGA, while maintaining full data rate capabilities.



### The X3 Product Group

The X3 PCI Express modules are industry standard XMCe cards which deliver performance with lower system cost

and less development effort than custom designs. Use the X3 XMCe modules in any PCI Express system or any XMCe compatible carrier card. Eliminate custom hardware by harnessing the power of PCI Express and customizable FPGA.

X3 modules have a PCI Express host interface delivering 180 - 350 MB/s data transfer rates, along with the flexibility of user-customizable FPGA signal processing. Board specific analog or digital I/O allows directly into the user-configurable Spartan 3 logic device. The supplied stock logic functionality allows the board to be used out-of-the-box as high-speed I/O board in which the large onboard RAM is configured as a virtual FIFO, to increase the instantaneous load-carrying capacity of the board to eliminate data overruns/underruns during real-time streaming.

Using the VHDL source code or MatLab board support package contained within the optional Framework Logic software package, you can readily customize the functionality of the FPGA to include real-time processing such as FIR and IIR filters on each channel, real-time FFT processing, ultra-fast feedback and control loops and much more. Use of Mat-Lab/Simulink with the MatLab board support package opens an entirely new range of realsolution possibilities. Importantly, this capability can be effectively used by anyone you need not be an FPGA or logic design maven to effectively develop custom logic solutions!



### The X5 Product Group

The X5 module family integrates high performance I/O with a Xilinx Virtex-5 FPGA computing core on 75x150 mm module

(IEEE1386) with a PCI Express interface. The Virtex-5 SXT FPGA provides up to 640 DSP48 elements combined with memory blocks and logic that support a complete DSP system on a chip. QDR SRAM and DDR2 DRAM memory pools provide the FPGA with deep, fast memory that is critical to implementing efficient signal processing algorithms and data acquisition.

Innovative's unique Velocia architecture provides up to 1 GB/s data streaming to the host that is flexible and extensible for all types of applications. It's fast and easy to use – allowing you to concentrate on your application work because it handles all the data flow and routing. You can freely mix high rate data streams with control and status making it easy to adapt to your application, yet still achieve the full GB/s data rate capabilities of the PCIe interface.

All X5 modules are architected to deliver high data throughput to the Host, along with





the flexibility of user-customizable FPGA signal processing. Board specific analog or digital I/O flows directly into the user-configurable Xilinx 5 logic device. The supplied stock logic functionality allows the board to be used out-of-the-box as a high-speed I/O board in which the large onboard DDR2 DRAM is configured as an enormous virtual FIFO data buffer. The QDR SRAM interface is a very high-speed local cache for custom algorithms running within the FPGA.

Eight PCI lanes equate to nearly unlimited 1200 MB/s sustained, real-world throughput. And due to the autonomy of the PCI architecture, this bandwidth is not diluted by activity of other PCI or PCI devices within the system each PCI slot operates independently and at full speed. But should it be necessary, the P16 interface can be used to provide another independent data path between FPGAs on multiple boards or carriers, further extending the communications capability of the module.

### COTS Solutions for High Performance IO

X5 and X6 modules enable new levels of performance in COTS systems and adds custom signal processing, data analysis and system features. It is easier than ever to achieve high performance because PCI Express architecture supports not only much higher data transfer rates, but also eliminates bottlenecks in the system using dedicated point-to-point links. And you'll be replacing custom hardware with an industry-standard PCI Express solution that gets you to market sooner with less cost.



### Customize COTS X5 and X6 Modules for Your Application

No other DSP solution can match the level of processing power and flexibility that the Virtex-5 and Virtex-6 FPGA core modules provide. MATLAB and RTL tools in the FrameWork Logic Board Support Packages enable you to customize the X5 & X6 modules for your application requirements and process real-time data at the IO, making system design more efficient and less complex. The MATLAB tools provide a powerful model-based design approach that allows you to go directly from MATLAB to

the hardware, radically reducing the time to implement complex signal processing functions. Or if you prefer, use the RTL tools when you need the power and flexibility of working in a high level language like VHDL or Verilog. The right tools for the job mean you get to market quicker.

### Software

Firmware and software are provided at no additional charge with each card which permit the board to be used immediately for the acquisition or generation of waveforms using all channels at full bandwidth, so that you can use the cards immediately, without programming, to characterize your analog signals or stimulate devices under test.

Turnkey data acquisition applications are provided for each module support data acquisition and logging. Tools are provided for data analysis, display and connection to MATLAB and Excel.

Innovative's Malibu Software Tools provide comprehensive and powerful software support C++ developers using Windows and Linux. In addition to the basic device drivers, the Malibu Tools have high performance data buffer management, signal processing and host application integration features that make application development and system integration straightforward and rapid.

X6 Module Features	Benefit
XMC Mezzanine Card	Compact IEEE 1386 card format (75x150mm)
XMC.3 PCI Express Module	Integrate into any VITA 42.3 PCI Express system
Virtex6 FPGA - SX315T/SX475T or LX240T	>300 GMACs/s (SX31595T) integrated with memory blocks and logic
4 GB LPDDR2	Real-time memory performance to 8 GB/s for FPGA data buffering and computation
PCI Express, 8 lane, gen2 interface	>3GB/s transfer rates to host eliminates custom hardware requirements
Analog and Digital IO integrated with FPGA	Real-time signal processing integrated with the IO
>4 GB/s dedicated secondary host interface	Tight, real-time host card integration with Serial RIO, Aurora and custom protocols





### X6-RX PCI Express XMC Module

Wireless Receiver, WLAN, WCDMA, WiMAX front end, RADAR, Medical Imaging, High Speed Data Recording and Playback, High Speed Servo Controls, IP Development

A/D

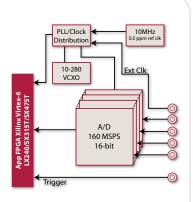
### Features

- Xilinx Virtex-6 SX315T/475T or LX240T
- 4 Banks of 1GB DRAM (4 GB total)
- Ultra-low jitter programmable clock
- Power Management features
- XMC Module (75x150 mm)

### Digital IO 32-bits (J16)

IP Cores for SDR 16-4096 DDC channels • PSK, FSK demodulation, OFDM receiver

Four 160 MSPS 16-bit A/D channels



# LILL **X6** 400m

### X6-400M PCI Express XMC Module

Ideal for Wireless Receiver and Transmitter, LTE, WiMAX Physical Layer, RADAR, Medical Imaging, High Speed Data Recording and Playback, IP development

### Features

- Two 400 MSPS, 14-bit A/D channels or
- Two 500 MSPS, 12-bit A/D channels • Two 500 MSPS, 16-bit D/A channels
- Virtex-6 SX315T/SX475T or LX240T
- 4 Banks of 1GB DRAM (4 GB total)
- Ultra-low jitter programmable clock
- Gen2 x8 PCIe 3 GB/s sustained transfer
- XMC Module (75x150 mm)
- 18-25W typical
- Conduction Cooling per VITA 20

### A/D

2 channels • 14-bit • 400 MSPS • >68 dB S/N @ 350MHz • +/-1V, 50 ohm, SMA

D/A

2 ch • 16-bit • 500 MSPS • 80 dB @ 400MHz or 1 ch • 16-bit • 1 GSPS

Digital IO: 33-bits (J16)

### IP Cores for SDR

16-4096 DDC channels • PSK, FSK mod/demod FFT 64K to 1M • OFDM receive and transmitter

Two 1.8 GSPS, 12-bit A/D channels or

+/-1V AC-Coupled 50 ohm SMA inputs

Front panel 64 single-ended or 32-bit LVDS

One 3.6 GSPS, 12-bit A/D channel



Wireless Receiver, WLAN, WCDMA, WiMAX front end, RADAR, Medical Imaging, High Speed Data Recording, IP development

A/D

Digital IO

44 bits (J16)

IP Cores for SDR

DDC for wideband channels

### Features

- Single channel interleaved @ 3.6GHz
- Virtex-6 SX315T/SX475T or LX240T
- 4 Banks of 1GB DRAM (4 GB total)
- Ultra-low jitter programmable clock
- Gen2 x8 PCIe 3 GB/s sustained transfer XMC Module (75x150 mm)
- 26W typical
- Conduction Cooling per VITA 20
- Ruggedization Levels for Wide
- Temperature Operation



**GSPS** 

### X6-1000 PCI Express XMC Module

Wireless Receiver, WLAN, WCDMA, WiMAX front end, RADAR, Medical Imaging, High Speed Data Recording and Playback, IP Development

### Features

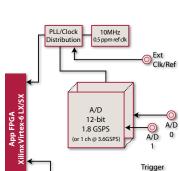
- Virtex-6 SX315T/SX475T or LX240T
- 4 Banks of 1GB DRAM (4 GB total)
- Ultra-low jitter programmable clock
- Controller for DACs
- Gen2 x8 PCIe 3 GB/s sustained transfer
- XMC Module (75x150 mm)
- 28W typical
- Conduction Cooling per VITA 20
- A/D

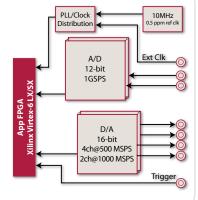
Two 1 GSPS, 12-bit A/D channels

+/-1V, AC or DC -Coupled, 50 ohm, SMA

- D/A Arbitrary Waveform Gen Memory
  - Two 1 GSPS, 16-bit DAC channels or
    - Digital IO: 32-bits (J16)
- Four 500 MSPS channels

IP Cores for SDR DDC, OFDM Rx/Tx, large FFTs





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A/D 14-bit 400 MSPS or 12-bit 500 MSF D/A 16-bit 500 MSPS or 1 ch @ 1GSPS

PLL

CLK/REF

Evt Clk/R



### X6-250M PCI Express XMC Module

Wireless Receiver, WLAN, WCDMA, WiMAX front end, RADAR, Medical Imaging, High Speed Data Recording and Playback, IP Development

### Features

- Virtex-6 SX315T/SX475T or LX240T
- 4 Banks of 1GB DRAM (4 GB total)
- Ultra-low jitter programmable clock
- Gen2 x8 PCIe option 3 GB/s sustained
- XMC Module (75x150 mm)
- 18-22W typical
- Conduction Cooling per VITA 20
- · Ruggedization Levels for Wide Temp

A/D Eight 310 MSPS, 14-bit A/D channels +/-1V, AC-Coupled, 50 ohm, SMC inputs D/A

xt Clk/Ref PLL A/D 14-bit 310 MSPS dd Trigger 0

CLK REF 10MHZ 0.5 PPM

320 VCX0

**210m** 

### X5-210M PCI Express XMC Module

Ideal for Wireless Receiver WLAN, WCDMA, WiMAX front end, RADAR, ECM, Electronic Warfare, High Speed Data Recording, Spectral Analysis, IP development

### Features

- Xilinx Virtex-5, SX95T
- 512 MB DDR2 DRAM
- 4 MB QDR-II SRAM
- 8 RocketIO private links, 2.5 Gbps/ea
- >1 GB/s, 8-lane PCIe Host Interface
- XMC Module (75x150 mm)
- PCI Express (VITA 42.3)

A/D

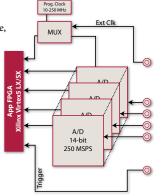
4 channels • 14-bit • 250 MSPS • +/-1V, 50 ohm, SMA inputs

D/A none

Digital IO 16-bits (J16)

• Power Management features

IP Cores for SDR 16-4096 DDC channels PSK, FSK demodulation, FFT 64K-1M





### X5-400M PCI Express XMC Module

Ideal for Wireless Receiver/Transmitter, WLAN, WCDMA, WiMAX front end, RADAR, ECM, Electronic Warfare, High Speed Data Recording and Playback, High Speed Servo Controls, Spectral Analysis, IP development

### Features

- Xilinx Virtex-5, SX95T FPGA
- 512 MB DDR2 DRAM
- 4 MB QDR-II SRAM
- 8 RocketIO private links 2.5Gbps/ea
- >1GB/s, 8-lane PCIe Host Interface
- · Power Management features
- XMC Module (75x150 mm)
- PCI Express (VITA 42.3)

2 ch • 16-bit • 500 MSPS • 80 dB @ 400MHz

### 33-bits (J16)

### IP Cores for SDR

16-4096 DDC channels • PSK, FSK demodulation FFT 64K to 1M



Front end signal processing ideal node for remote IO and distributed processing systems such Remote Radio Head (RRH) applications

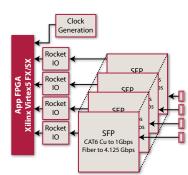
### Features

- Xilinx Virtex-5, SX95T/FX100T
- SX95T: 640 DSP48E elements
- FX100T: dual PowerPC processors
- 512 MB DDR2 DRAM
- 4 MB QDR-II SRAM
- 8 RocketIO private links, 2.5
- Power Management Features
- XMC Module (75x150 mm)
- PCI Express (VITA 42.3)

### Front Panel IO

16-bits (J16)

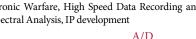
4 SFP ports • Fiber Optic or Copper Interface Up to 3.125 Gbps D/A none Digital IO





com

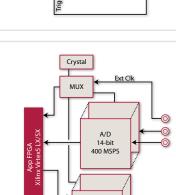
**X**5 400m



2 channels • 14-bit • 400 MSPS • >68 dB S/N @ 350MHz • +/-1V, 50 ohm, SMA in & out

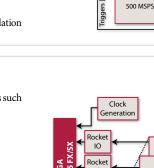
D/A

Digital IO



DAC

16-bit







### X5-G12 PCI Express XMC Module

Ideal for Wireless Receiver, WLAN, WCDMA, WiMAX front end, RADAR, Medical Imaging, High Speed Data Recording, IP development

A/D

### Features

- Xilinx Virtex-5, SX95T or LX155T
- 512MB DDR2 DRAM
- 4MB QDR-II SRAM

• PCI Express (VITA 42.3)

- 8 Rocket IO private links, 2.5 Gbps each
- Power Management features

• Integrated FFT for up to 256K FFTs

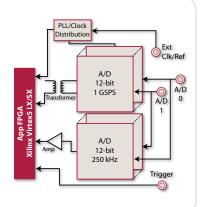
- +/-1V, 50 ohm, DC or AC coupled inputs
- >1 GB/s, 8-lane PCIe Host Interface
- XMC Module (75x150 mm)
- D/A none

### Digital IO

Front panel 64 single-ended or 32-bit LVDS 33 bits (J16)

One 2 GSPS, 12-bit A/D single channel mode

Two 1 GSPS, 12-bit A/D channels or



PLL/Clock

Distribution

Fxt Clk

A/D

8-bit

1.5 GSPS



an an an an an ar

rx

### **X5-GSPS PCI Express XMC Module**

Ideal for Wireless Receiver, WLAN, WCDMA, WiMAX front end, RADAR, Electronic Counter Measures (ECM), Electronic Warfare, High Speed Data Recording, Spectral Analysis, IP developments

2 channels • 8-bit • to 1500 MSPS

1 channel • 8-bit • to 3000 MSPS

### Features

- Xilinx Virtex-5, SX95T FPGA
- 512 MB DDR2 DRAM
- 4MB ODR-II SRAM
- 8 Rocket IO private links, 2.5 Gbps/ea
- >1 GB/s, 8-lane PCIe Host Interface
- · Power Management features
- XMC Module (75x150 mm)
- PCI Express (VITA 42.3)

(National ADC08D1520) +/-1V, 50 ohm, SMA D/A

none

A/D

- Digital IO

16-bits (J16) IP Cores for SDR 16-4096 channels

# X5-RX PCI Express XMC Module

Ideal for Wireless IF Receiver and Processor, Multi-channel RADAR

### Features

- Xilinx Virtex-5 SX95T
- 640 DSP48E elements
- 512 MB DDR2 DRAM
- 4 MB QDR-II SRAM
- 8 RocketIO private links, 2.5 Gbps/ea
- >1 GB/s, 8-lane PCIe Host Interface
- Power Management features
- XMC Module (75x150 mm)
- PCI Express (VITA 42.3)

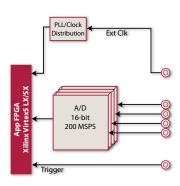
+/-1V input range D/A none Digital IO

4 channels • 200MSPS • 16-bit

16-bits (J16)

A/D

IP Cores for SDR 16-4096 channels FFT 64K-1M





### **X5-TX PCI Express XMC Module**

Ideal for Wireless Transmitter, High Speed Arbitrary Waveform Generation, Exact channel alignment MIMO transmit applications

A/D

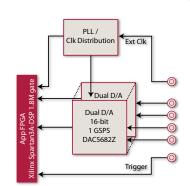
none

- Xilinx Virtex-5 SX95T • 640 DSP48E elements • 512 MB DDR2 DRAM • 4 MB QDR-II SRAM • 8 RocketIO private links, 2.5 Gbps/ea • >1 GB/s, 8-lane PCIe Host Interface · Power Management features • XMC Module (75x150 mm)
- PCI Express (VITA 42.3)

D/A
2 ch • 1 GSPS • 16-bit
4 ch • 500 MSPS • 16-bit
+/-1V output range

Digital IO: 16-bits (J16)

**IP** Cores OFDM Tx



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### X3-2M PCI Express XMC Module

Ideal for Multichannel sensor interface, Neuro-physical instrumentation, High speed motion recording, Spectral Analysis, RADAR

### Features

- Xilinx Spartan3A DSP, 1.8M gate FPGA
- 50 ohm, differential inputs
- Continuously acquire 12 simultaneous
- channels at 10 MSPS to module memory
- Stream to system mem at up to 220MB/s
- 4MB SRAM

### A/D

12 channels of 10 MSPS, 16-bit simultaneously sampling A/D

-110 dB noise floor, 91 dB SFDR

Low latency SAR converters

- D/A
- · Sample clock is external or
- programmable, low jitter PLL
- Framed, software or external triggering
- none
- Digital IO 44-bits (J16)

Ext Clk PLL AD9510 VCO REF 10-280 MHz 100MHz Š A/D Connector **MDR68** og Devi AD7625/6 16-bit 10 MSPS Front Panel DIO [11:0] Triggers [1..0]

PLL/Clock

A/D

16-bit

25 MSPS

Linear LTC2203

[riaaers [1..0]

Ext CI

Gain (

n U

MDR68



### X3-10M PCI Express XMC Module

Ideal for Multichannel sensor interface, Neuro-physical instrumentation, High speed motion recording, Spectral Analysis, RADAR

### Features

- Spartan 3A, DSP 1.8Mgate FPGA
- 4MB SRAM
- Programmable PLL timebase
- Framed, software/external triggering
- · Log acquisition timing and events
- · Power Management features • XMC Module (75x150 mm)
- PCI Express (VITA 42.3)

### A/D

8 channels • 16-bit • 25 MSPS (simultaneous) +/-2V, +/-1V, +/-0.4V, +/-0.2V input ranges differential, high impedance inputs

D/A

none

- - Digital IO 44-bits (J16)

### X3-25M PCI Express XMC Module

Ideal for Wireless Receiver/Transmitter, Stimulus-response, Electronic Counter Measures (ECM), High Speed Servo Controls, Arbitrary Waveform Generation, Spectral Analysis, RADAR

### Features

- Spartan 3A, DSP 1.8Mgate FPGA
- 4MB SRAM
- External/Programmable PLL timebase
- Framed, software/external triggering
- Log acquisition timing and events
- 16-bit front panel DIO LVDS/TTL
- · Power Management features
- XMC Module (75x150 mm)
- PCI Express (VITA 42.3)

A/D

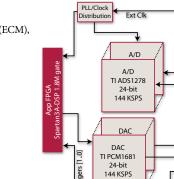
2 channels • 16-bit • 105 MSPS +/-2V, +/-1V, +/-0.2V input ranges

### D/A

2 channels • 16-bit • 50 MSPS +/-2V output range

### Digital IO

44-bits (J16) 16-bits front panel





### X3-A4D4 PCI Express XMC Module

Ideal for Servo Controls, Stimulus-response measurements, Arbitrary Waveform Generation

### Features

- · Low Latency I/O for Servo Apps
- Spartan3A DSP, 1.8M gate FPGA
- 4MB SRAM
- External/programmable PLL clocking
- -115 dB noise floor

• 16 bits front panel IO

- · Framed, software/external triggering
- · Log acquisition timing and events

- · Power Management features

D/A

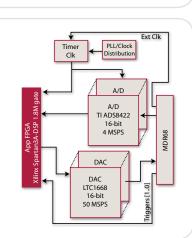
4 channels • 16-bit • 4 MSPS

+/-10V, +/-5V, +/-2.5V, +/-1.25V input differential, high-impedance inputs

4 channels • 16-bit • 50 MSPS +/-10V output range

### Digital IO 44-bits (J16)

16-bits front panel





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### X3-DIO PCI Express XMC Module

Ideal for Pattern Generation, Custom Digital Interfaces for Remote IO, Digital Controls

A/D

none

D/A

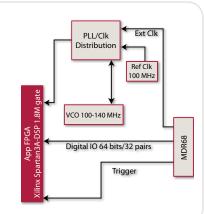
none

Digital IO

44 bits (J16)

Front panel 64 single-ended or 32-bit LVDS

- Features
- 100 MHz signal to FPGA using LVDS
- 50 MHz LVCMOS signal rates
- 400 MB/s LVDS capture/play to SRAM
- Optional on-card termination
- Spartan3A DSP, 1.8M gate FPGA
- External clocking and triggering
- External/Programmable PLL timebase
- Framed, software/external triggering
- · Log acquisition timing and events



### X3-SD PCI Express XMC Module

Ideal for Vibration Measurement, Audio and Acoustic Testing, Data acquisition

### Features

- >110 dB SFDR >105 dB S/N
- -135 dB noise floor
- Sample rates up to 216 ksps
- Programmable oversampling modes
- Xilinx Spartan3, 1M gate FPGA
- 4MB SRAM
- External/Programmable PLL timebase
- Framed, software/external triggering
- · Log acquisition timing and events
- Power Management features
- A/D 16 channels • 24-bit • 216 kHz +/-10V differential inputs

D/A none

- Digital IO
- 44-bits (J16)

### X3-SD16 PCI Express XMC Module

Ideal for Wide Dynamic Range Acoustic and Vibration Measurements, Spectral Analysis, Audio Waveform Generation

### Features

- Spartan 3A, DSP 1.8Mgate FPGA
- 4MB SRAM
- External/Programmable PLL timebase
- Framed, software/external triggering
- · Log acquisition timing and events
- 16-bit front panel DIO LVDS/TTL
- Power Management features

### • XMC Module (75x150 mm)

- PCI Express (VITA 42.3)

### A/D

16 channels • 16-bit • 144 KSPS 2/10/20V input ranges

- - 16 channels 24-bit 144 KSPS +/-2V output range

### Digital IO



**SD16** 

# X3-SDF PCI Express XMC Module

Ideal for Vibration Measurement, Audio and Acoustic Testing, Data acquisition

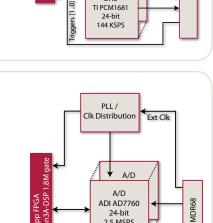
A/D

D/A

none

### Features

- >110 dB SFDR @ 625 ksps
- >105 dB S/N @ 2.5 MSPS
- -130 dB noise floor
- · Programmable output resolution and sample rates up to 20 MSPS
- Programmable filters
- Xilinx Spartan3, 1M gate FPGA
- 4MB SRAM
- External/Programmable PLL timebase
- Framed, software/external triggering
- Log acquisition timing and events



24-bit

2.5 MSPS

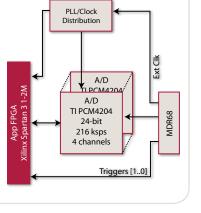
Triggers [1..0]

4 channels • 24-bit • Fast Sigma-Delta

(simultaneous up to 20 MSPS)

+/-5V differential inputs

Digital IO 44-bits (J16)



Ext Cll

A/D

A/D

TI ADS1278 24-bit

144 KSPS

DAC

DAC

**MDR68** 

PLL/Clock

stribution

Innovative Integration

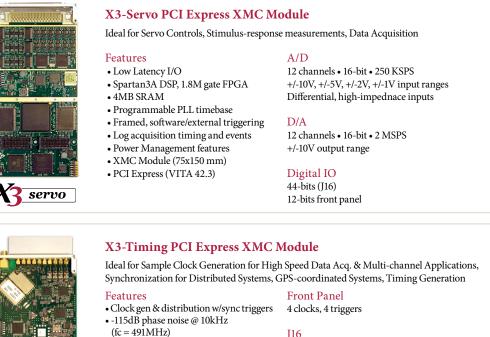
44-bits (J16) 16-bits front panel

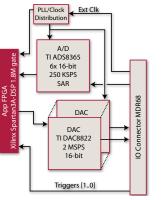
D/A

25

aa







GPS



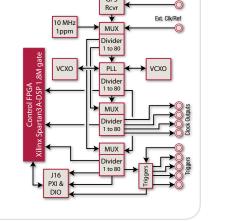
- 0.3 ps jitter RMS
- Synchronize to GPS or local clocks
- 1M to 1 GHz Output Range
- Clock ref is GPS, ext. or on-card 10 MHz
- 10MHz, 280 PPB on-card reference
- Integrated GPS (clock ref & time stamp)
- PXI master clock source with PXI
  - adapter for all sys clocks and triggers

### J16

PXI DSTARA, B, C, 10 MHz reference, 8 triggers

Digital IO 29 bits (J16)

- · Supports large channel count systems
- with multiple card synchronization



Antenna



# **Carrier/Adapter Boards**

Adapt PMC/XMC/FMC Modules to Desktop, Notebook, Compact PCI, PXI and OpenVPX Systems

### PMC & XMC Carrier Cards

Innovative Integration's convenient carrier cards allow a single PMC, XMC or FMC module to be used in any standard 32 or 64 bit PCI, CompactPCI, desktop PCI-Express or 3U Open VPX slot. Alternately, one module or more XMC modules may be remotely located near the unit under test and connected via a cable up to ten meters in length to a PC to create a 200 MB/s local-area data acquisition network. Ideal for production and test environments!

Adapters for PCI Express XMC modules (VITA42.3) provide special support for Innovative X3, X5 and X6 module families. Features such as shared clocks and triggers, communications links and access to J16 connector makes the modules easier to integrate into any system.

### FMC Adapters

These adapters allow use of standard FMC modules within 3U OpenVPX systems and desktop PCs featuring standard PCI Express expansion slots.



**PEX6-COP** PCI Express Desktop/Server Coprocessor with Virtex-6 FPGA computing core and FMC IO site



VPX6-COP openVPX 3U OpenVPX Coprocessor with Virtex-6 FPGA computing core and FMC IO site

PMC Adapters

These adapters allow use of standard PMC modules within a desktop PC featuring standard PCI or PCI Express expansion slots.



PMC to PCI Adapter Fast, Simple PCI Adaptation for PMC and PTMC Modules



### PMC to PCI Express Adapter

Fast, Simple PCI Express Adaptation for PMC and PTMC Modules

XMC Adapters

These adapters allow use of standard XMC modules within a desktop PC or expansion chassis, cPCI chassis or 3U VPX system.



XMC Adapter for 3U OpenVPX openVPX Adapter allows a single width XMC module to be used in a 3U OpenVPX slot Rugged Conduction or Air Cooled XMC Adapter with IPMI Support



### XMC to PCI Express Adapter (8-lane) XMC x8 lane to PCI Express x8. Supports private high speed RIO links to other cards J16 breakout connector



XMC to PCI Express Adapter XMC x1 lane to PCI Express x1 J16 breakout connector Trigger and clock inputs





XMC x4 lane to CompactPCI-X, 64 bit, up to 133MHz Supports PXI XMC to PCI Adapter

XMC to CompactPCI Adapter

XMC to PCI Adapter XMC x4 lane to PCI-X, 64-bit 133 MHz J16 breakout connector Trigger and Clock inputs

CPEX Adapters

These adapters allow use of standard XMC modules tethered to a desktop PCI featuring PCI Express expansion slots or to a laptop PC with an ExpressCard slot.



PCI Express X1 Cable Adapter Transparent PCI Express Cable Adapter Express-Card for notebooks



CPEX8 -PCI Express X8 Cable Adapter Transparent PCI Express Cable Adapter



**CPEX4 Hub - 4-lane PCI Express Hub** Use with Innovative PCIe X1 Cable adapters

CPEX4-PCI Express X4 Cable Adapter Transparent PCI Express Cable Adapter





### PCI Express X1 Cable Adapter Transparent PCI Express Cable Adapter



Innovative Integration | 805.578.4260 | www.innovative-dsp.com



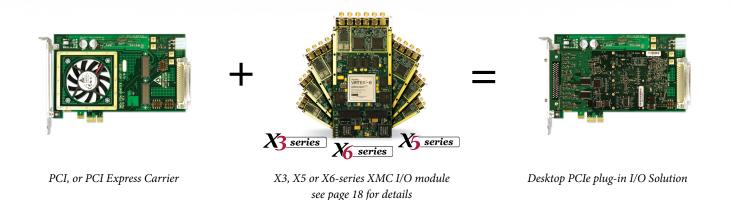
# **PCI Express Boards**

Intelligent, Customizable I/O High Performance I/O and FPGA Core

### PCI Express Boards

Our X3, X5, and X6 XMC modules are also usable as PCI Express Desktop PC Plug-in boards.

Mounting an XMC module atop our XMC PCIe adapter creates an industry-standard desktop PCI Express plug in card which can deliver performance with lower system cost and less development effort than custom designs. Use in any PCI Express based desktop or industrial PC system. Eliminate custom hardware by harnessing the power of PCI Express and a customizable FPGA. Read more about our wide array of XMC modules on page 18.



Mounting an FMC module atop our PEX6-COP PCIe adapter creates an industry-standard desktop PCI Express plug in card which can deliver performance with lower system cost and less development effort than custom designs. Use in any PCI Express based desktop or industrial PC system. Eliminate custom hardware by harnessing the power of PCI Express and customizable I/O and FPGA. Read more about our wide array of FMC modules on page 6.



Innovative VITA57-compatible FMC Modules see page 6 for details

Desktop PCIe plug-in I/O Solution



PEX6-COP FPGA Coprocessor/FMC Carrier

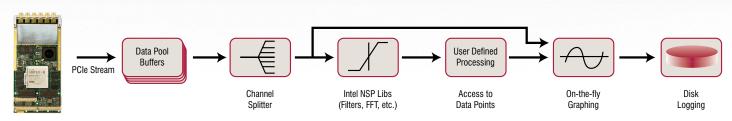


# **Innovative Software Toolsets**

**Design Fast - Get to Market Faster!** 

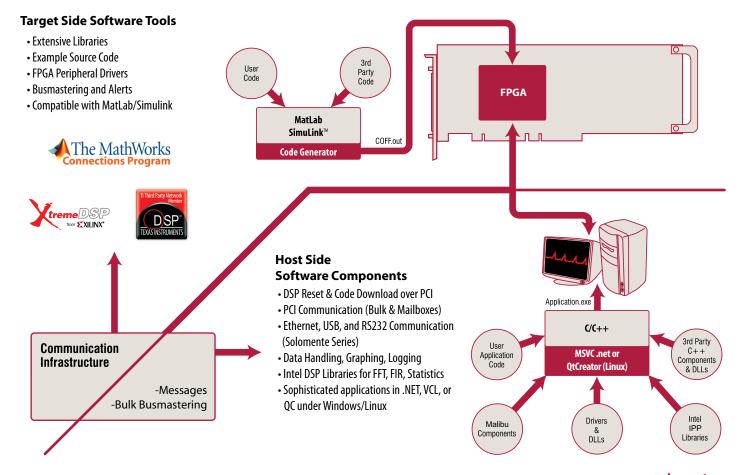
### Accelerate System Development with Practical Board-Level Software

With over 25% of our engineering staff working on software, Innovative Integration invests heavily in board-level software support. With every board, we ship a large, complete set of libraries, utilities, and program source code examples that greatly accelerate end-users development. Skip the arduous, low-level hardware and driver programming and jump straight into YOUR application!



### MALIBU - Host-Side Software Tools for Practical Board Config & Com

The host-side software tools, written in C++, allow simple control of and communication with the DSP hardware: boot method, message send/receive, data bidirectional stream control. In addition, a unique, user-friendly and powerful set of components accelerate deployment of data-intensive application: data buffer management, channelization, dynamic viewing/graphing, file logging. It includes Intel's fastest and greatest signal processing libraries, the Intel Performance Primitives.



Innovative Integration

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# **Malibu Libraries**

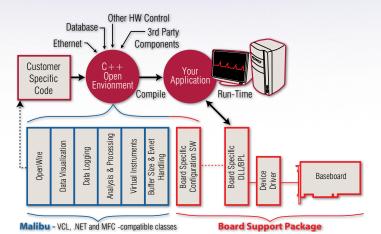


Ultimate Performance Signal Processing & Data Acquisition Libraries Rapid Application Development

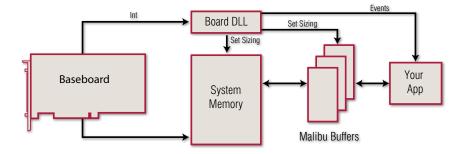


Malibu – Rapid Application Development for Signal Processing & Data Acq. Malibu is a powerful, feature-rich software library designed to meet the challenge of developing software capable of high-speed data flow and real-time signal analysis on the PC. Malibu adds high-performance data acquisition and data processing capabilities to Microsoft Visual C++ .NET or Borland (CodeGear) Developers Studio applications with a complete set of functions that solve data movement, analysis, viewing, logging and fully take advantage of the object-oriented nature of C++. The full data sheet may be downloaded from www.innovative-dsp.com/products/malibu.htm

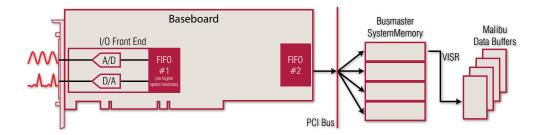
Malibu supports command and control plus data transfer using Innovative's new DSP and data acquisition platforms. It incorporates board support packages comprised of a low-level board device driver (Windows or Linux) and portable libraries which allow full hardware configuration and control from within a C++ application or DLL. The ability to call Malibu functions within a static or dynamic library makes it easy to create custom board interfaces to allow utilization of Innovative Integration DSP or data acquisition products from within third-party graphical environments such as LabView or MatLab.



Malibu automatically manages and dispatches all hardware real-time events and works with the hardware to smoothly flow data and messages between the target and the host application. The library is optimized for low-latency, high-speed data flow and computation at every stage throughout the application.



Hardware data flow uses an advanced data buffering system that allows the PC to achieve high rates while sustaining the overall demands of real-time applications. Where appropriate, multiple stages of data buffering are used to mitigate the rate of interrupt requests. Data flows through driver allocated contiguous physical memory to support sustained real-time demands for data movement, while minimizing data latency normally incurred with large data buffers. This approach is superior to the typical scatter/gather system because it eliminates the overhead associated with managing non-contiguous data buffer pools.





### Malibu is a large collection of portable C++ code containing classes organized into the following general categories:

### **Buffer Classes**

The buffer classes provide access to common vector signal processing functions and analysis functions needed in real-time data acquisition and control applications or for post-processing operations. Most of the classes utilize MMX and SIMD-optimized code using the Intel Performance Primitive libraries that offer the highest performance.

The Malibu buffer classes implement copy-on-write to maximize performance. Malibu's internal, proprietary buffer manager has been designed for optimal real-time performance with minimal runtime heap thrashing and superfluous copy operations.

### Analysis Classes

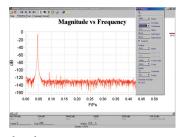
The analysis classes provide access to common DSP algorithms and analysis functions. Most of the components are MMX and SIMD optimized code from the Intel libraries that offer the highest performance.

### **Digital Signal Processing Classes**

In addition to the standard DSP classes listed below, base classes are provided from which you can readily derive to create custom filters and signal generators.

### Signal Generation Classes

High-speed generation of Gaussian, Sinusoudal, triangular, square and random signals.



### Data Visualization Classes

Develop data graphs. Multiple channels may be simultaneously displayed on a single graph for applications like strip chart recorders and oscilloscopes. Full control of the graph type, scaling and point marking make it easy to develop sophisticated displays. Interactive features allow the user to measure

data during acquisition. Binview is a powerful data graphing and analysis tool that you can directly interface to your application as a post-processing analysis tool. That allows you to view all types of data sets of virtually unlimited size. You can quickly switch viewing between time domain and frequency domain options and see analysis statistics like standard deviation, signal to noise ratio, THD and SINAD. Scrolling and data search features allow you to quickly scan through large data sets.

### Data Recording and Playback Classes

Malibu provides built-in support and extensive examples for data logging and playback applications. You can record data to and playback data from Windows file system disks at up to 400 Mb/s with the components supplied with Malibu. You can also record to network drives for system integration.

### System Components

A useful set of system components saves development time. Classes and functions are provided for precision profiling and delays, automatically marshal event processing into the foreground thread. A stop watch allows for quick application profiling while other components give direct access to data in RAM, facilitate the numeric display of data arrays and simplify the use of registered Windows messages.

### System Functions

File presence and size detection.

### **Resource Sharing Classes**

Most real-time applications involve use of resources which must be cooperatively-shared amongst multiple threads. The classes below facilitate thread creation and thread-safe code and data sections.

### Multithreading Support Classes

Abstract base class plus standard derivatives which signal a semaphore or fire an user-controllable event.

### **Baseboard** Classes

These classes provide direct access to each of the Innovative board level products via the supplied device drivers. Methods are provided for COFF file downloading, logic loading, configuration, triggering, real-time bi-directional data flow and manipulation of board-specific features such as DDCs or other embedded signal processing capabilities.

### Hardware Support Classes

These classes encapsulate the behavior of common hardware features available on Innovative hardware. For instance, boards featuring analog or digital I/O peripherals employ a precision, user-programmable conversion clock source. Clock objects are provided to allow full control of these timebases in within application programs.

### Hardware Register Classes

Many Innovative board-level products employ user-reprogrammable FPGAs, whose behavior may be changed via custom VHDL code. A complete assortment of Register objects are provided to allow convenient bit and field manipulation within user-defined registers.

### Information Classes

These classes act as information containers. For instance, boards featuring multiple analog channels allow enabling of individual channels. The ChannelInfo class provides detailed information about the resultant data format flowing from the device.

### **Communications Classes**

In addition to high-rate, block-oriented data flow, messages objects are supplied which are more convenient when passing parametric information or commands between Host and Target.

### Timebase Classes

Classes supporting programmatic control of the flexible sample clocks incorporated on Innovative board-level products.

### String Classes

Classes for manipulation of lists and vectors of strings, binary and format conversion.

### **Bit Manipulation Functions**

These optimized functions implement commonly-needed bit-manipulation algorithms, such as bit-reversal) in a highly-efficient manner.

### Arithmetic Functions

These methods perform commonly-needed arithmetic algorithms in a highlyefficient manner, such as base-2 log, ceiling, floor, ones detection, etc.





# **Software Support**

# Design Fast - Get to Market Faster! Utilities & Turnkey Applications

### Be Productive From Day One!

Every board support toolset includes utilities and turnkey applications that allow end-users to immediately focus all their resources on their application. Enormous resources are delivered free of charge and give our customers the means to get their systems to market faster.

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### Loop Applet

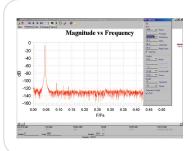
The supplied Loop example supports use of the FPGA as a real-time coprocessor. Test data sets may be streamed to the FPGA at full PCI Express bus rates. Custom firmware within the FPGA processes the incoming stream and sends the resultant data back to the host via PCIe. Transmit and receive test vectors are stored independently for pre/post processing or visualization. Indispensable for acceleration of complex DSP algorithms, such as those produced by Matlab/Simulinks

Board # Open Close	
Logic Image	
	(88)
Update Logic	
Write Verily	
Collocation Cold Version: 0	GOLDEN BODT
Log	

### VSProm Applet

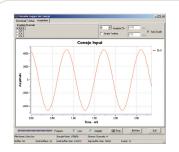
The supplied VsProm utility supports in-field Flash firmware reprogramming on the X5 and X6 -series XMC modules as well as the configuration memory on the PEX6-COP and VPX6-COP coprocessor/carriers.

The flash update operation can be controlled via the graphical user interface to the left or embedded within C++ application code using calls in the supplied Malibu libraries.



### BinView - View and Analyze Your Captured Data

Display and Analyze data graphically Zoom, scroll through large files Time and Frequency Domain Fully portable Export and import data with analysis packages



### Snap/Wave - Sophisticated Data Acquisition and Playback, out-of-the-box

Powerful, flexible data acquisition turnkey application Includes host and DSP program source code Fully exploits A/D & DAC channels, busmastering and mailbox messaging A solid foundation serving as reference design



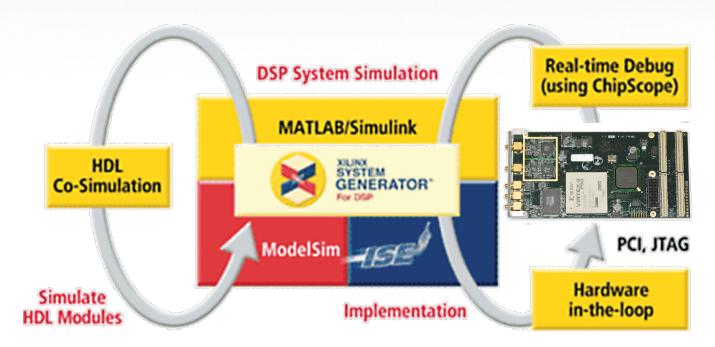


# Matlab & Xilinx System Generator

MatLab/FrameWork VHDL Support

### Develop DSP in MATLAB Simulink ... then go straight to hardware!

Using MATLAB Simulink with Xilinx System Generator, develop DSP systems in the MATLAB environment then run them directly on hardware, all with bittrue, cycle-true results that bring the real world data and hardware into MATLAB. With Innovative Integration's FrameWork Logic and MATLAB board support packages, you can quickly integrate signal processing into the hardware without lengthy, complex coding.



Libraries of signal processing algorithms and hardware functions, written specifically for implementation in logic, allow you to build high-speed signal processing applications and test them under MATLAB. Support for real-time data capture and signal generation gives you the power to use MATLAB to analyze real in-system performance at full rate.

When used with Innovative Integration's FrameWork Logic, you can mix HDL with MATLAB for unique features, or vice versa. Completely flexible, extensible tools give you the power to create your application, with all its unique features without compromise.

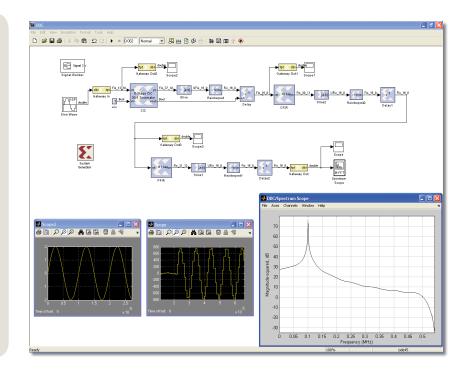
Product	FPGA	FrameWork VHDL	MATLAB
X6 Series XMC Modules	Virtex-6 - LX/SX	•	•
PEX6-COP / VPX6-COP	Virtex-6 - LX/SX	•	•
X5 Series XMC Modules	Virtex-5 - LX/SX	•	•
X3 Series XMC Modules	Spartan 3A-DSP, Spartan 3 - 1 & 2M	•	•
UWB PMC Module	Virtex-2 Pro - VP40/50	•	•
TX PMC Module	Virtex-2 Pro - VP40/50	•	•
DR PMC Module	Virtex-2 Pro - VP40/50	•	•

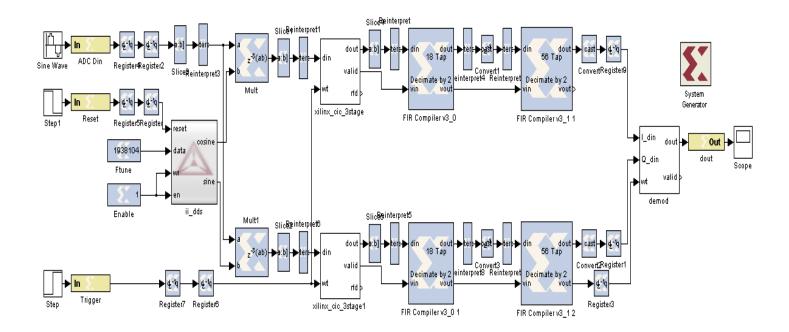


# **Matlab & Xilinx System Generator**

### Innovative Board Support Package Features

- Integrates hardware directly into MATLAB Simulink
- Examples demonstrate hardware use under MATLAB
- FrameWork Logic system in VHDL with example logic
- Function libraries for hardware & signal processing
- IO interfaces A/D, DAC and digital IO
- Triggers and timers
- Data buffers very large FIFOs, pattern generation and capture
- System communications host DSP, PCI, and external





SDR Receiver with 180 MSPS digitizing, DDCs and PSK demodulation implemented in MATLAB on X5-210M

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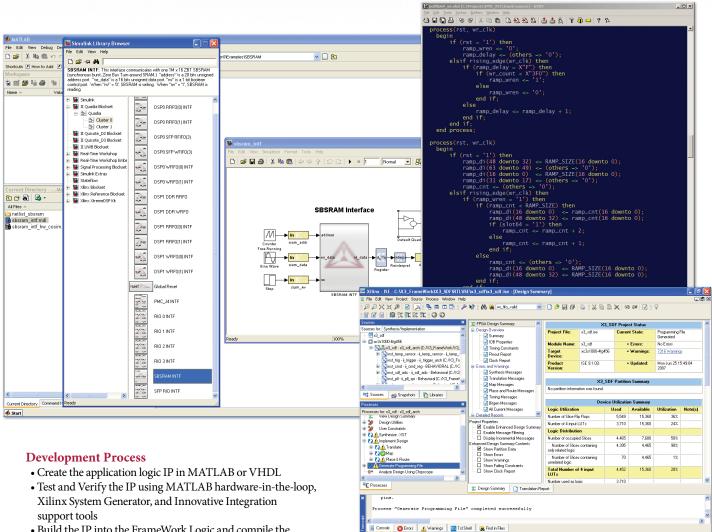


# **FrameWork Logic**

# Logic Development for real-time signal processing and control in FPGAs

The FrameWork Logic tools provide comprehensive support for customizing FPGA firmware to add signal processing, controls and data analysis to Innovative Integration hardware products. Whenever your application calls for the highest level of real-time performance, adding DSP or custom controls to the FPGA on the card is a great solution.

The FrameWork Logic BSPs support FPGA logic development in MATLAB and RTL for many of Innovative Integration products. FrameWork Logic helps you complete your project sooner by providing pre-written and verified IP cores and logic for hardware interfaces, data buffering and DSP.



• Build the IP into the FrameWork Logic and compile the project in Xilinx ISE



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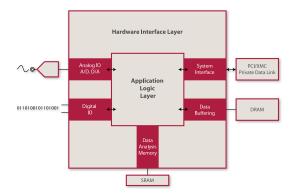
### **RTL Board Support Packages (BSP)**

### Shorten your development time by integrating your code into the FrameWork Logic

- Pre-written and tested hardware interface components
- · Sensible data-flow design is easy to modify
- Velocia and Vita packet data host interface is flexible, extensible, and fast
- Command Channel host interface for status/controls is easy to adapt

### **Each BSP contains**

- FrameWork Logic application example in VHDL
- Library of logic components
- Xilinx ISE projects and ModelSim Testbench
- Open-source code with documentation



Application logic is added to the FrameWork Logic inside a hardware interface layer

	IP Core	Supported Products	Function
Memory Control	ii_ddr_pg	X5, X6	Memory controller for pattern generation using DDR2 DRAM
	ii_sram_intf, ii_sram32_intf	X3	Flexible interface to 16 or 32 bit ZBT SRAM. Supports transfer rates to 250 MB/s
	ii_mq_sram, ii_mq_sram32	X3	Multiple-queue controller for ZBT SRAM
	ii_128mq	X5, X6	Multiple-queue controller for DDR2 DRAM supports up to 4 GB/s transfer rates.
	ii_ddr_fifo_mq	PMC	Multiple-queue controller for DDR DRAM supports up to 1.2 GB/s transfer rates.
	ii_qdr_sram	X5, X6	Flexible interface to 16 or 32 bit QDRII SRAM. Supports transfer rates to 2.5 GB/s
VITA-49 Packets	ii_vita_framer	X6	Creates VITA packets
	ii_vita_deframer	X6	Extracts payload from VITA packets
	ii_vita_router	X6	VITA packets routing
Bus Interface	ii_pcie_intf	X5, X6	PCle interface for 8 lanes implementing Velocia packet system. 1 GB/s sustained rates
	ii_link	X3	64-bit data link to PCl Express interface controller supporting 250 MB/s.
	ii_cmd_channel	X3	Host system command and control data channel.
Velocia Packet	ii_packetizer	X3, X5, X6	Creates data packets for PCI Express/PCI system interface and software.
System	ii_deframer	X3, X5, X6	Parses and routes data packets for PCI Express/PCI system interface and software.
10	A/D and DAC interfaces	X3, X5, X6	Design-specific A/D and DAC interfaces for data acquisition and control.
System Monitor	ii_temp_sensor	X3	Monitors system temperature and provides power controls.
	ii_monitor	X5, X6	Monitors system temperature, FPGA voltages and provides power controls.
	ii_alert	X3, X5, X6	Monitors sys op & provides timestamped packets (overflow, overrange and triggering)
Data Acquisition	ii_trigger	X3, X5, X6	Data acq controls for software/external triggering (framed capture mode & decimation)
	ii_offgain	X3, X5, X6	Error compensation and correction for analog IO.
Communications	ii_aurora	X5, X6	Communications link using Aurora with subchannels supports 300MB/s.

### **Supported Tools**

Code Development

• Xilinx ISE using

VHDL/Verilog

Xilinx System Generator

Simulation • Modelsim Signal Processing • MATLAB, Simulink Debug • Xilinx Chipscope



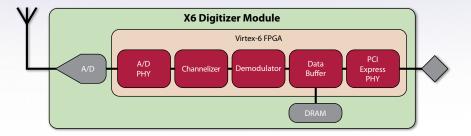
# **Wireless IP Cores**

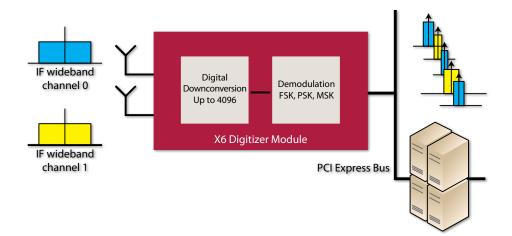
High performance FPGA cores for channelization, downconversion, and demodulation



### IP Cores for SDR Applications

Innovative Integration provides IP focused on Software Digital Radio IP cores. These cores provide essential front-end signal processing for digital down-conversion, channelizing, and demodulation which are the core of any modern SDR application. These cores are also available integrated into X5-series and X6-series XMC modules, providing off-the-shelf solutions for wireless, RADAR and instrumentation applications.



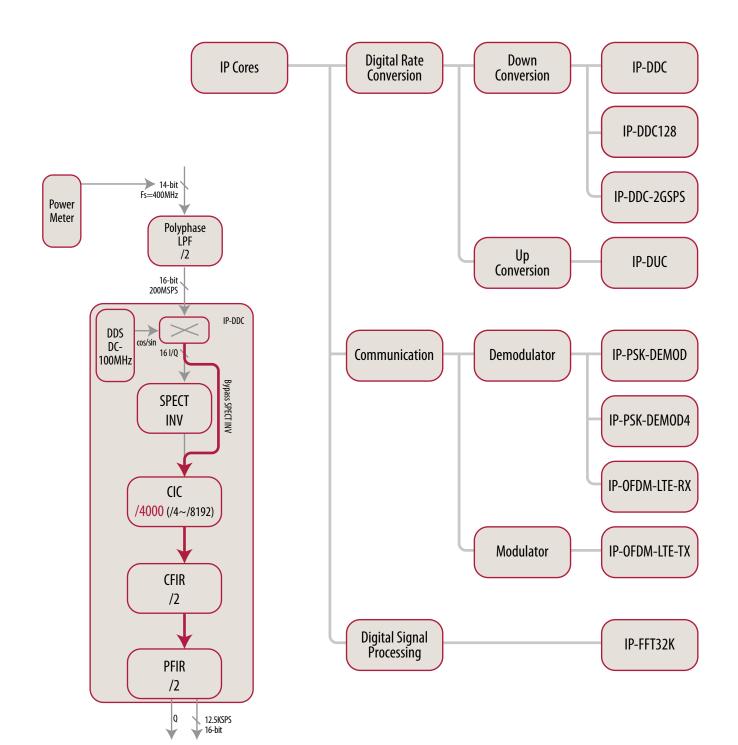


Embedding channelizers and demodulation into FPGAs increases channel density, improves flexibility, and reduces system cost.

Description	
N=2,4,8, pi/4,; Net version	
MSK,FSK,GMSK	
Single channel wideband DDC, decimation 2-32768	
Eight Independent Channel Digital Downconversion Core for FPGA	
Single channel DDC core for data rate up-to 500 MSPS	
128 Channel Digital Downconversion Core for FPGA	
	N=2,4,8, pi/4,; Net version MSK,FSK,GMSK Single channel wideband DDC, decimation 2-32768 Eight Independent Channel Digital Downconversion Core for FPGA Single channel DDC core for data rate up-to 500 MSPS



# **Wireless IP Cores**







Visit www.innovative-dsp.com for datasheet downloads & online pricing!

### Innovative Integration 741 Flynn Road

Camarillo, California 93012

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