FrameWork Logic

Development Tools for High Speed Signal Processing in FPGAs

Features

- MATLAB and VHDL Board Support Packages
- Comprehensive hardware support and tools for signal processing
- Hardware inteface layer design structure allows rapid integration of application-specific code
- Designed to support real-time signal processing and data acquisition
- Reference designs illustrating hardware use

Advantages

- Accelerate design, test and verification using MATLAB and VHDL tools
- The flexibility of open-source VHDL, complemented by the power and ease of use MATLAB
- Graphical block diagram design
- Component-based RTL design
- Go directly from MATLAB Simulink model to hardware using bit-true, cycle-true logic IP cores
- Integrate the power and ease of use of MATLAB into hardware testing and verification
- Use MATLAB Simulink for signal generation, analysis and display with live hardware
- Real-time support while using MATLAB

Functions

- VHDL Board Support providing IO, data buffering and system interfaces
- MATLAB Board Support Packages for Velocia DSP and PMC hardware (see availability list)
- Logic IP cores for IO, data buffering, system interfaces, communications and signal processing
- Simulation with ModelSim and MATLAB

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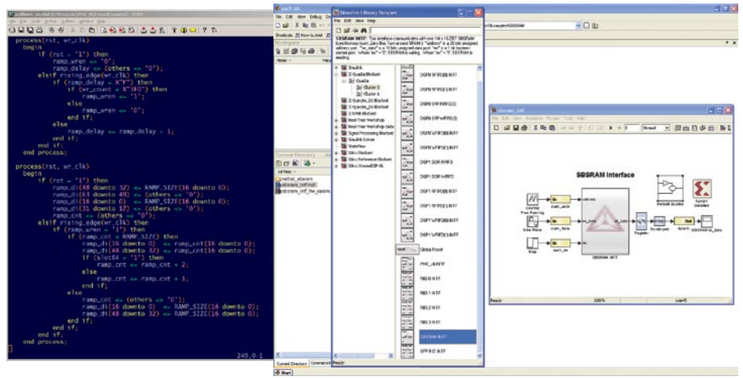
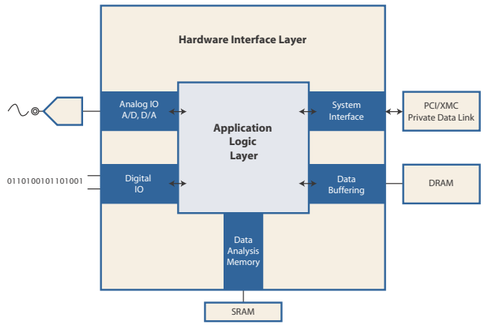
Overview

The FrameWork Logic tools provide comprehensive support for FPGA signal processing development in MATLAB and RTL for Innovative Integration products. The logic development cycle is shortened by building application logic within the FrameWork Logic hardware layer using pre-written and verified IP cores. The MATLAB tools provide a powerful graphical block diagram environment for hardware-in-the-loop and support real-time data generation and analysis. The RTL tools complement the MATLAB environment and provide the flexibility of a high-level language. The tested high level signal processing can be seamlessly integrated with VHDL in the same project, allowing you to work with the tools best suited for the job.



Development Process

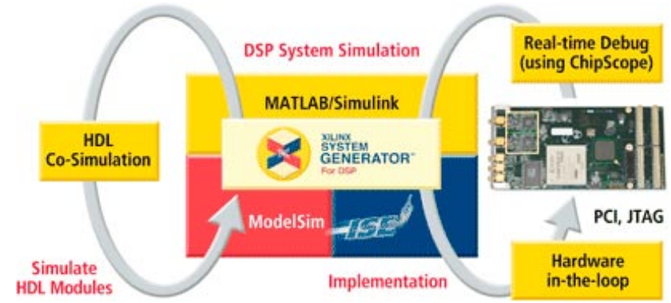
- ***Create*** the application logic IP in MATLAB or VHDL
- ***Test and Verify*** the IP using MATLAB hardware-in-the-loop and Innovative support tools
- ***Build*** the IP into the FrameWork Logic and compile the project in Xilinx ISE



Application logic is added to the FrameWork Logic inside a hardware interface layer

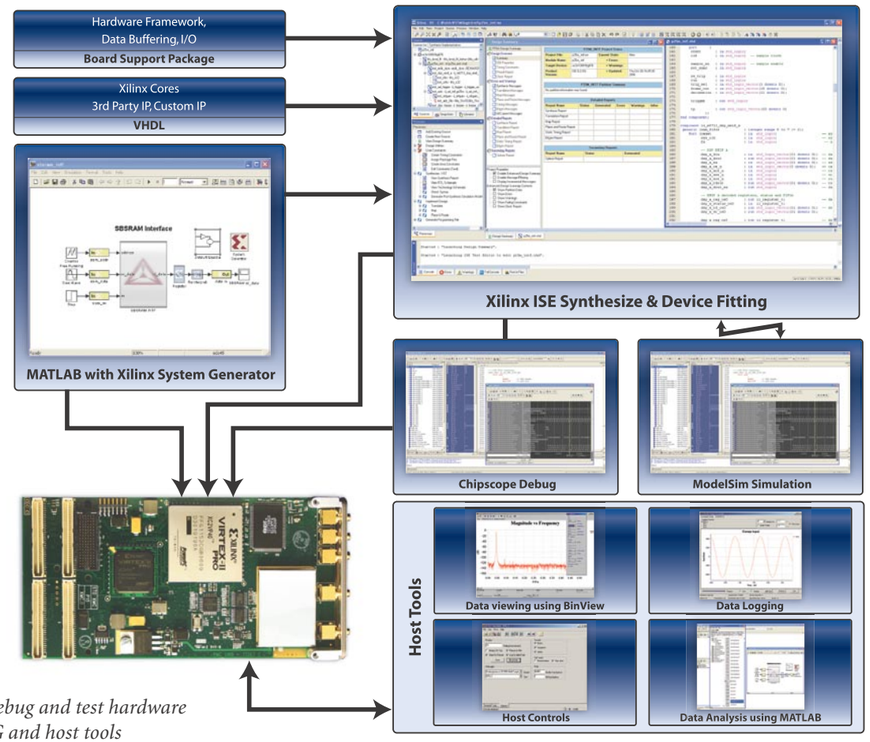
MATLab Development

- The most rapid and efficient way to develop signal processing IP for logic
- Direct hardware co-simulation from within the MATLAB environment
- Board Support Packages allow MATLAB to be used with live hardware for data generation, analysis, display
- Board Support Packages use Xilinx System Generator to directly compile MATLAB Simulink block diagrams into logic cores.
- JTAG interface to hardware allows in-system testing and verification.
- Real-time support to collect snapshots of high speed data or generate real-time signals
- Cores developed under MATLAB integrate easily into FrameWork Logic for fully embedded logic applications



VHDL Development Process

The VHDL development process enables you to create application logic using IP cores from Xilinx, Innovative and 3rd parties and integrate those cores into the hardware interface layer. In many cases, the signal processing application can be simply inserted into the data flow between the IO to the data buffering. The logic is fully customizable using the VHDL source code provided with the FrameWork Logic.



Develop, debug and test hardware using JTAG and host tools

Innovative Integration
real-time solutions

Hardware Support IP (Partial List)

Hardware Control Cores	Function
Virtual FIFO	Implements a FIFO using DDR DRAM memory buffer
Multi-queue FIFO	Implements multiple FIFO queues in DDR DRAM memory buffer
Pattern Generator	Implements a dynamically loadable pattern generator for DDR DRAM capable of >500 MB/s sustained operation
SRAM Controller	Provides high speed synchronous SRAM interface
Packetizer	Packetizes data for system interfaces
Deframer	Unpacketizes data from system interface
J4 Link	Implements a data link over PMC J4 connection to base cards capable of >350 MB/s
SFP Data link	Provides an SFP data link interface (Quadia)
RIO Data Link	Provides a RIO link interface between FPGAs with flow control
DSP interfaces	Interface cores for standard TI DSPs ('6416, '6713)
DDC Interface	Interface to TI GC5016 quad-channel DDC devices
Quadrature Decoding	Interface to industry-standard quadrature encoders
Sigma Delta DAC	Sigma Delta modulator and controls implements a DAC function. External analog filter is required.
Triggering Controls	Snapshots, external triggering, decimation

DSP Cores	Function
Digital Downconversion	20 channels DDC operating at up to 208 MHz
Spectral Inverter	Real-time spectral inversion
FFT	Radix-2 FFT, 32 to 8K record lengths
FIR Filters	Support via Xilinx Corelib and Matlab. The number of taps that may be implement for real time operation depends on sample rate, logic utilization and logic clock rate.
CIC Filters	Support via Xilinx Corelib and Matlab.

Supported Hardware Platforms

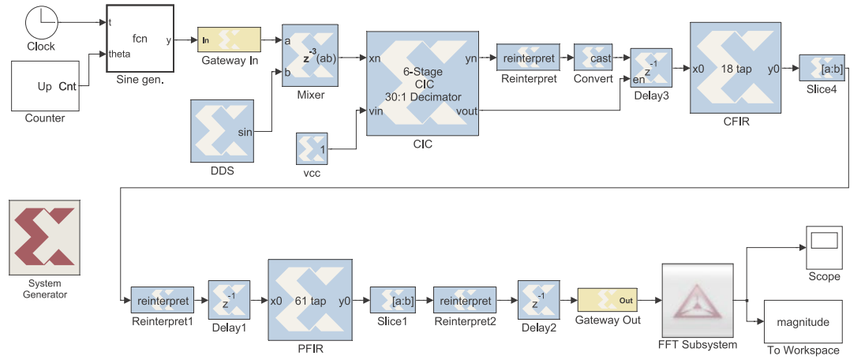
Hardware Platforms with MATLAB BSP	Features	Application	Available
Quixote	6U compact PCI card with Xilinx Virtex2 2M/6M, TI '6416 1GHz DSP, two 105 MSPS A/Ds, two 105 MSPS D/A, 4MB SRAM for FPGA	Software Digital Radio, high speed pulse digitizing	Now
Quadia	6U compact PCI card with two Xilinx Virtex2 Pro VP40 FPGAs, 2MB SRAM and 32MB DRAM per FPGA, four TI '6416 DSPs @1GHz, dual PMC/XMC sites, dual SFP ports, PLLs, J5 rear terminal IO, high speed J4 interface	Multi-processor DSP/FPGA platform with dual PMC/XMC sites	Now
PMC UWB	PMC module with 2x 250 MSPS, 12-bit A/D, Xilinx VP40 FPGA, 2MB SRAM, 64 MB DRAM, PLL and clocking features, PCI 64/66 bus, 4 Rocket IO lanes for XMC 42.0, high speed J4 interface	Software Digital Radio, high speed digitizing	Now
PMC TX	PMC module with 4x 1 GSPS, 16-bit DACs, Xilinx VP40 FPGA, 2MB SRAM, 64 MB DRAM, PLL and clocking features, PCI 64/66 bus, 4 Rocket IO lanes for XMC 42.0, high speed J4 interface	SDR, arbitrary waveform generation	11/06
PMC DR	PMC module with 4x 125 MSPS, 14-bit A/D, Xilinx VP40 FPGA, 16-channels of digital downconversion using four TI GC5016 devices, 2MB SRAM, 64 MB DRAM, PLL and clocking features, PCI 64/66 bus, 4 Rocket IO lanes for XMC 42.0, high speed J4 interface	SDR	12/06

FrameWork Logic

Application Examples

Forty Channel Digital Radio Receiver (DRR)

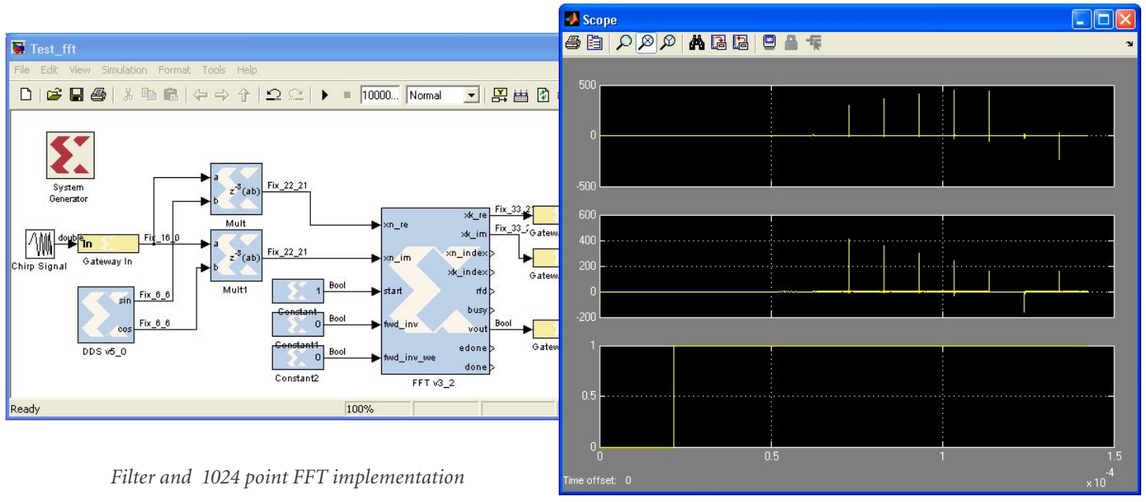
- GSM Receiver
- Implements forty channels of DRR using a Quadia DSP card and two PMC UWB modules
- 130 MSPS or 208 MSPS digitizing rate.
- Dynamically tunable with channel filtering and data buffering features
- MATLAB Simulink model for DRR implements directly into logic firmware
- Fully reconfigurable design implemented in VHDL and MATLAB
- Support software demonstrates DRR control and data capture



From MATLAB to hardware using FrameWork Logic and Xilinx System Generator tools

FFT Analysis

- Easy implementation and analysis of an point FFT
- Configurable within MATLAB to modify the functionality
- Board support package provides direct hardware interface to MATLAB
- Pre-verified IP cores from Xilinx and Innovative provide data handling and analysis
- Graphical block diagram design using MATLAB Simulink
- Click of a button deployment of embedded DSP application using Innovative Integration board support package (BSP) and Framework logic



Filter and 1024 point FFT implementation

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FrameWork Logic Packages

The Framework Logic support packages support application logic development with comprehensive support for each hardware platform.

VHDL Board Support Package

- Source files in VHDL
- Constraints
- Xilinx ISE project
- Testbench and Modelsim project
- Example logic
- On-line help for example logic

MATLAB Board Support Package

- Simulink library with hardware support
- Board-specific infrastructure logic
- Examples

Required Tools for RTL

- Synthesis: Xilinx XST. Other tools that produce netlists readable by the Xilinx tools for place and route may also be used.
- Device Fitting : Xilinx tools including PACE, Floorplanner, Constraints Editor, FPGA Editor
- Timing Analysis : Xilinx Timing Analyzer, ModelSim
- Simulation: ModelSim. The PE version is recommend for larger designs.
- Debug: Xilinx Chipscope Pro

MATLAB Development

These tools are required for MATLAB development *in addition* to the RTL tools

- MATLAB version 7.x or higher
- Xilinx System Generator
- Xilinx JTAG cable: Platform USB or Parallel Cable IV
- FrameWork Logic

Support and Application Engineering

- Comprehensive manual and on-line help for each FrameWork Logic Board Support Package
- Applications engineering support via telephone, email and web forum

Ordering Information

The logic and FrameWork Logic User Guide may be downloaded free of charge from Innovative Integration website (registration required)

Innovative Integration | 805.578.4260 | www.innovative-dsp.com