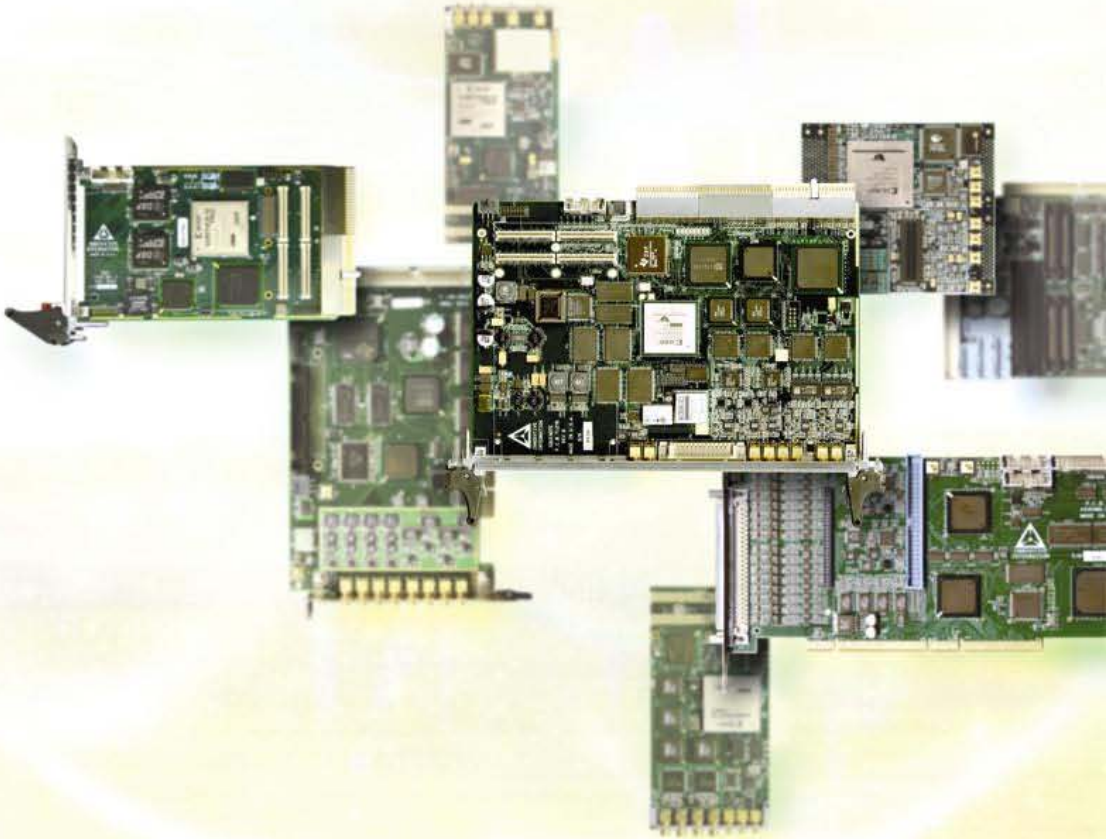
FrameWork Logic and MATLAB Board Support Package



Dan McLane
Billy Kao

Innovative Integration

FrameWork Logic and MATLAB Products

Innovative Integration
... real time solutions!

- Innovative Integration offers
  - FrameWork Logic for traditional VHDL design using Xilinx ISE software
  - Support for MATLAB/Simulink and Xilinx System Generator based designs
  - Extensive II VHDL IP cores
- Results
  - Rapid application development
  - Smooth integration of custom logic in II Framework
  - Real time testing and debugging of algorithms using ChipScope Pro and MATLAB/Simulink

Innovative Integration
... real time solutions!

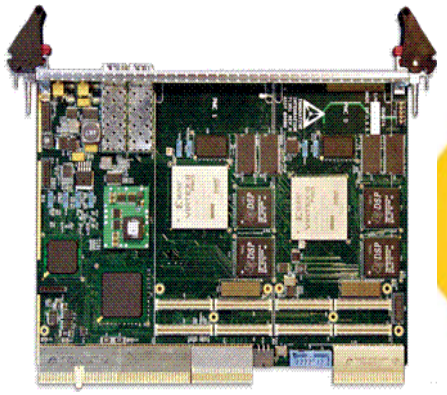
MATLAB Board Support Package

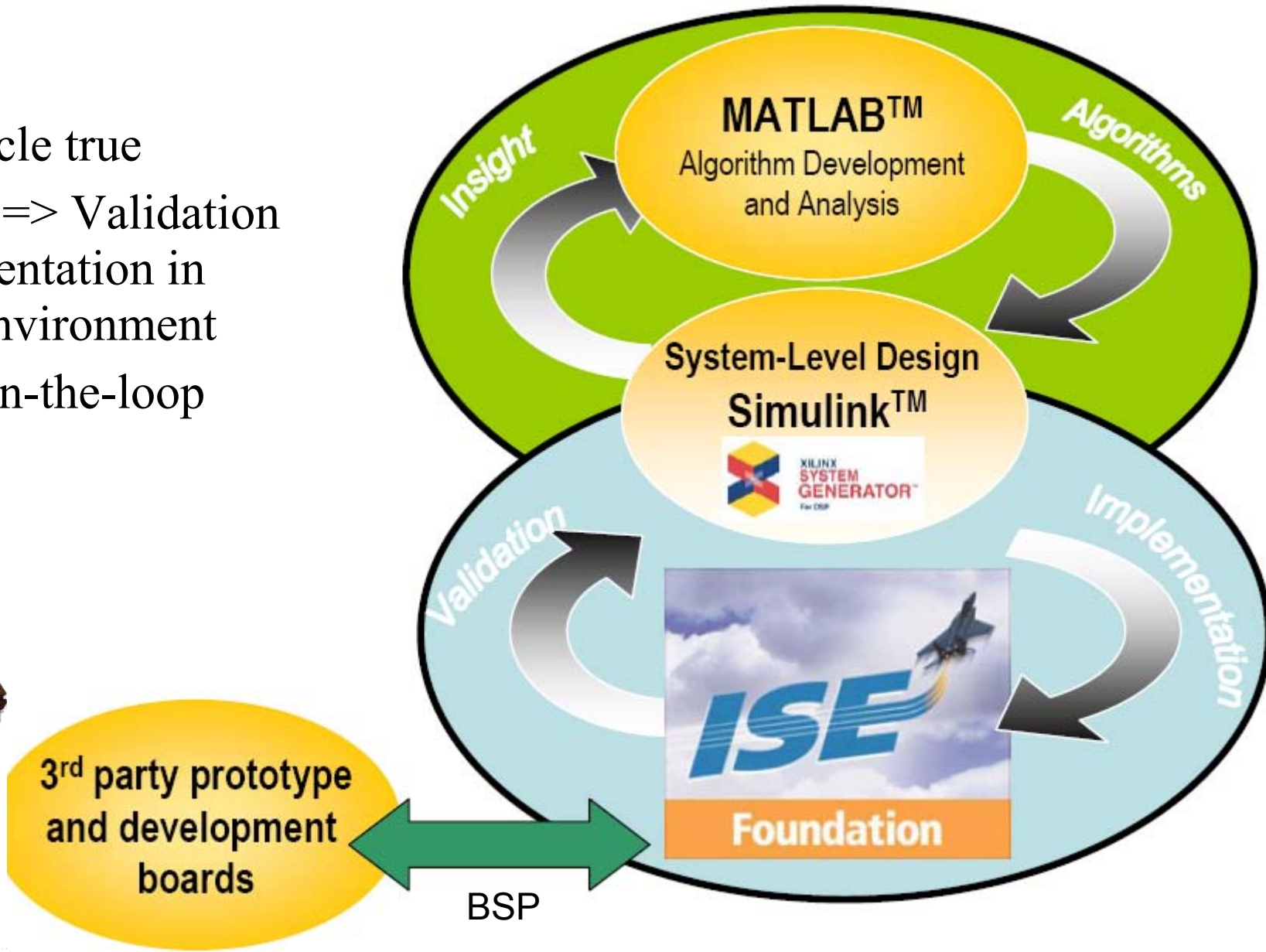
Bridge to the Real World - System Generator/Simulink

Innovative Integration
... real time solutions!

Features

- Bit true, cycle true
- Simulation => Validation => Implementation in Simulink environment
- Hardware-in-the-loop





Start Your Design in Simulink

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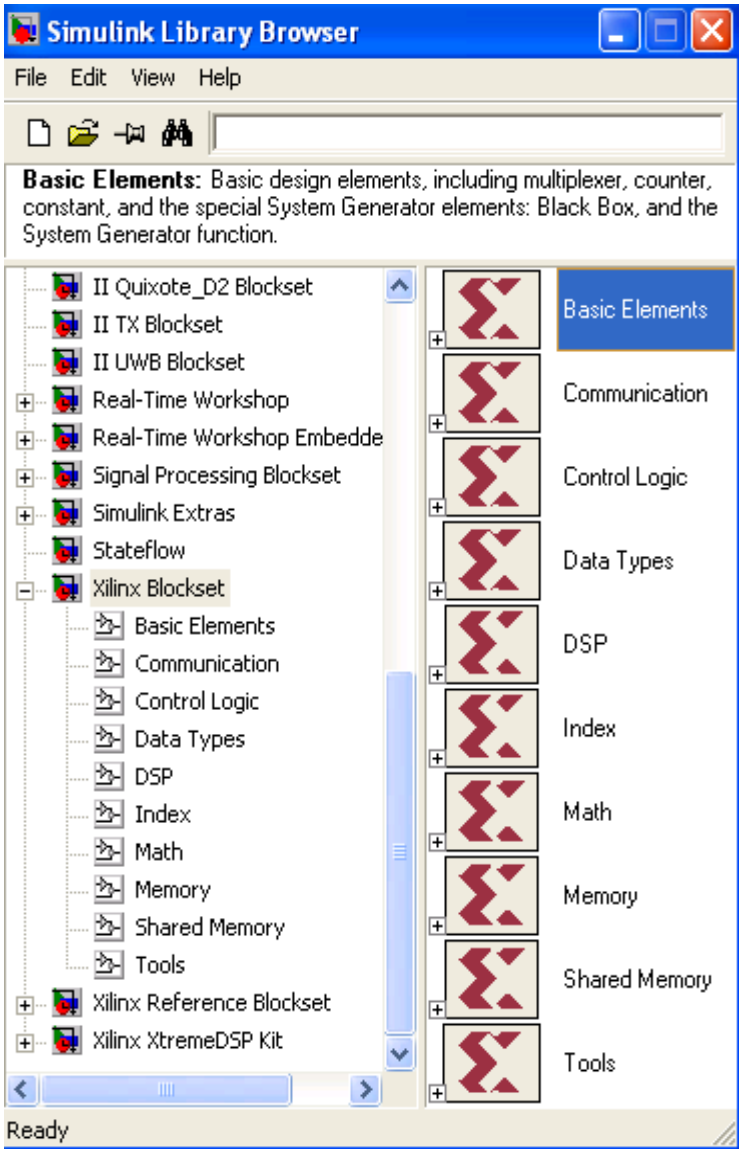
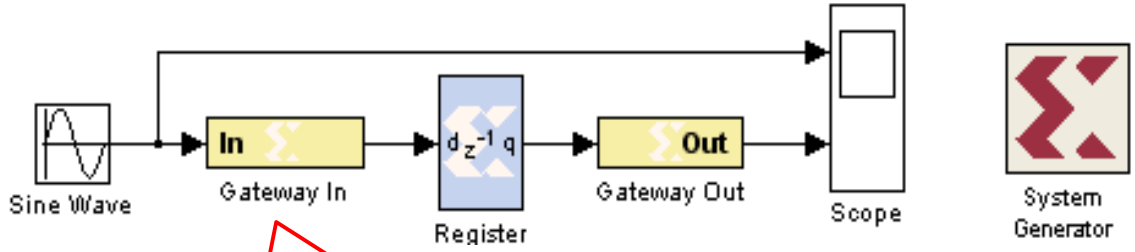
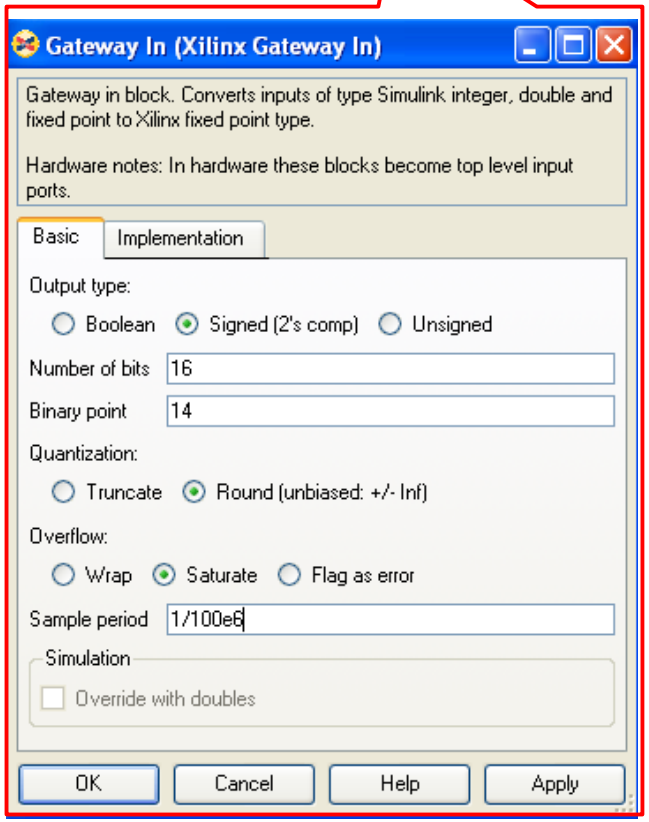
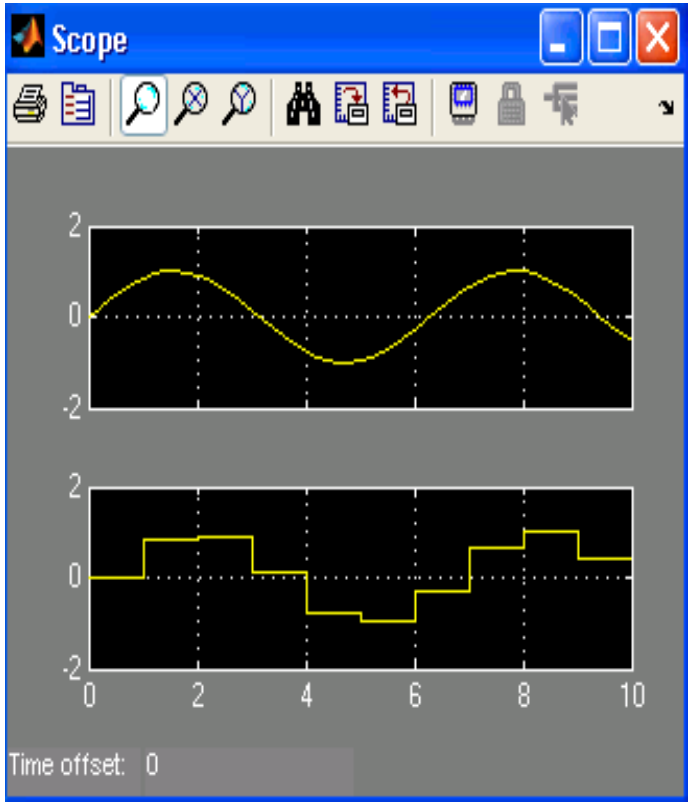
... real time solutions!



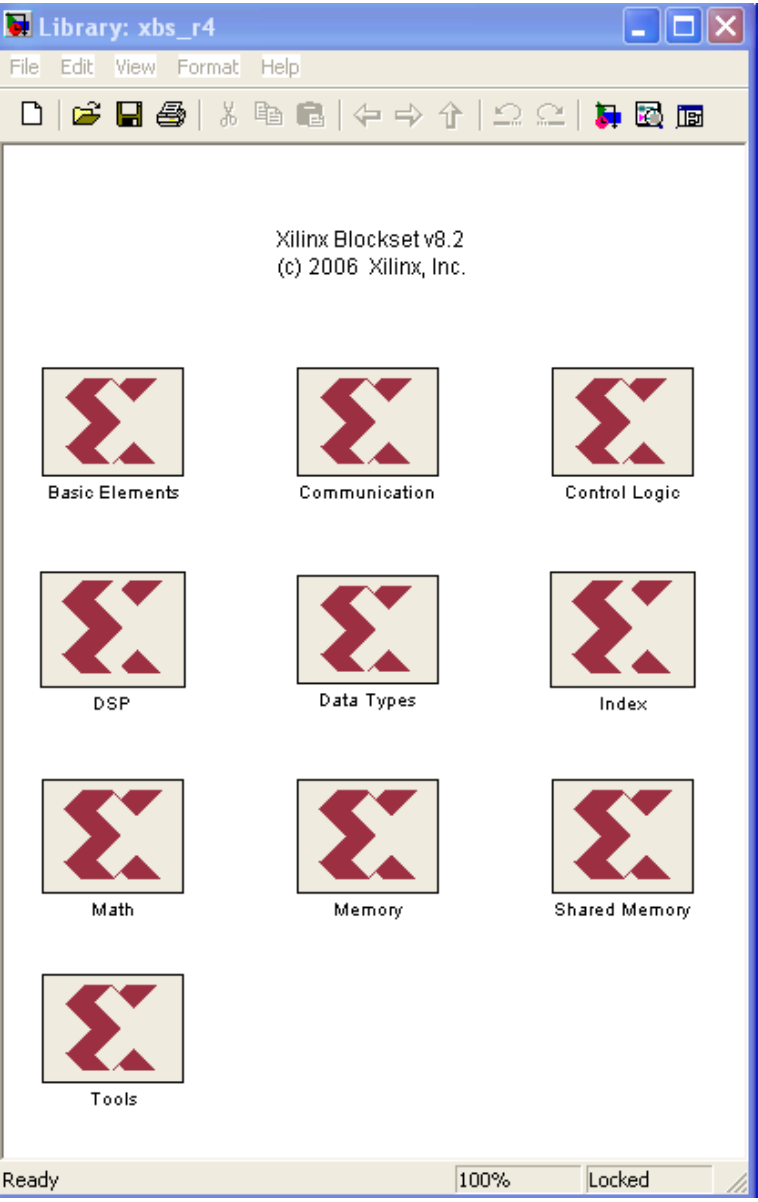


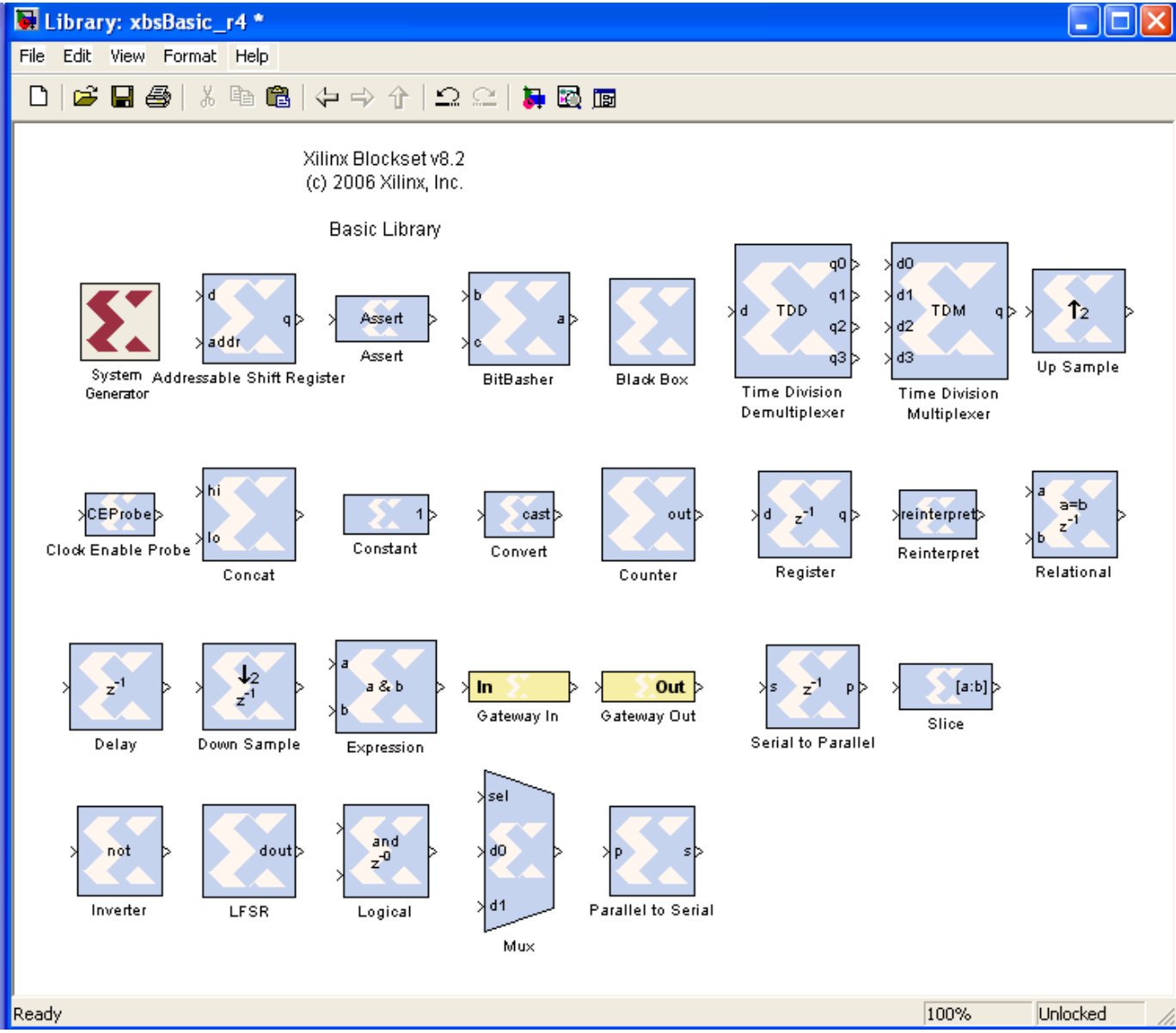




Xilinx System Generator

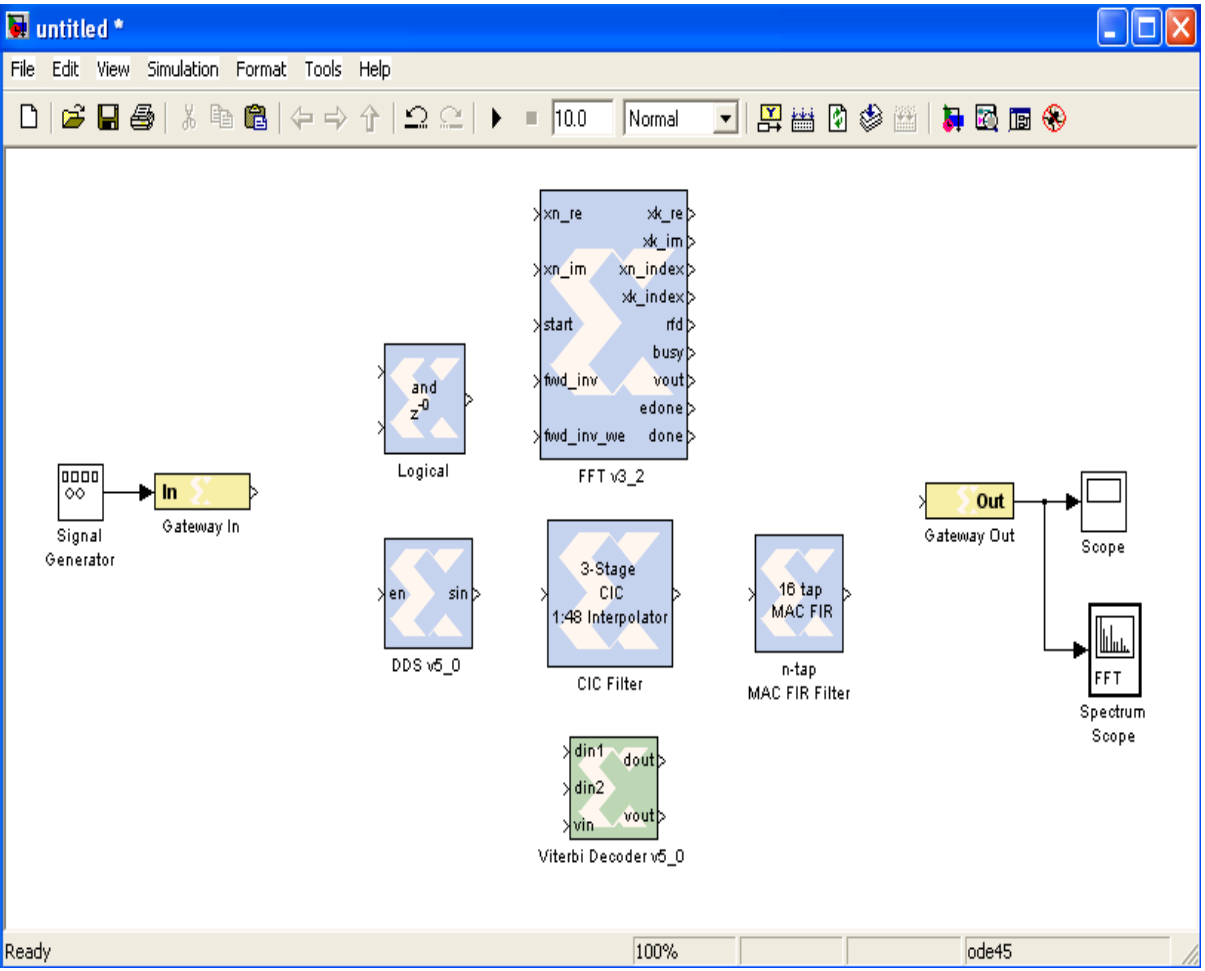
Innovative Integration
... real time solutions!



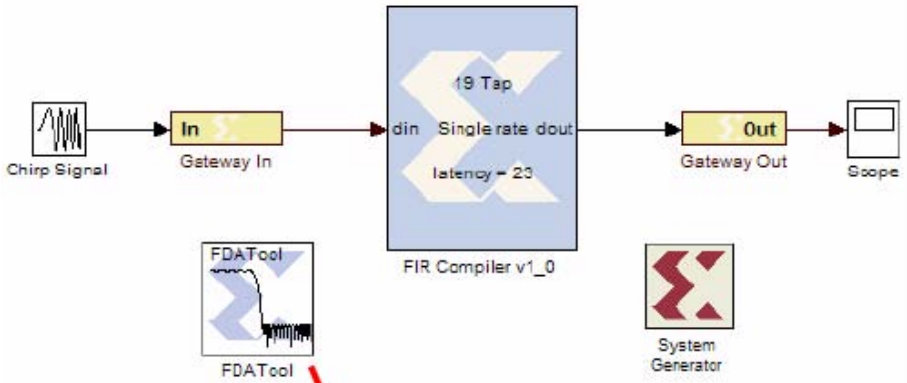


System Modeling in Simulink

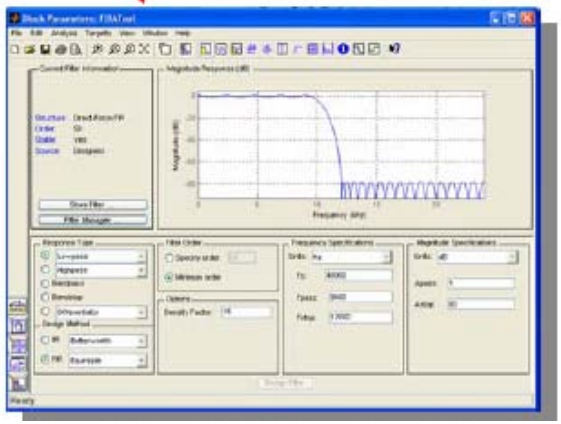
Innovative Integration
... real time solutions!



FIR Compiler



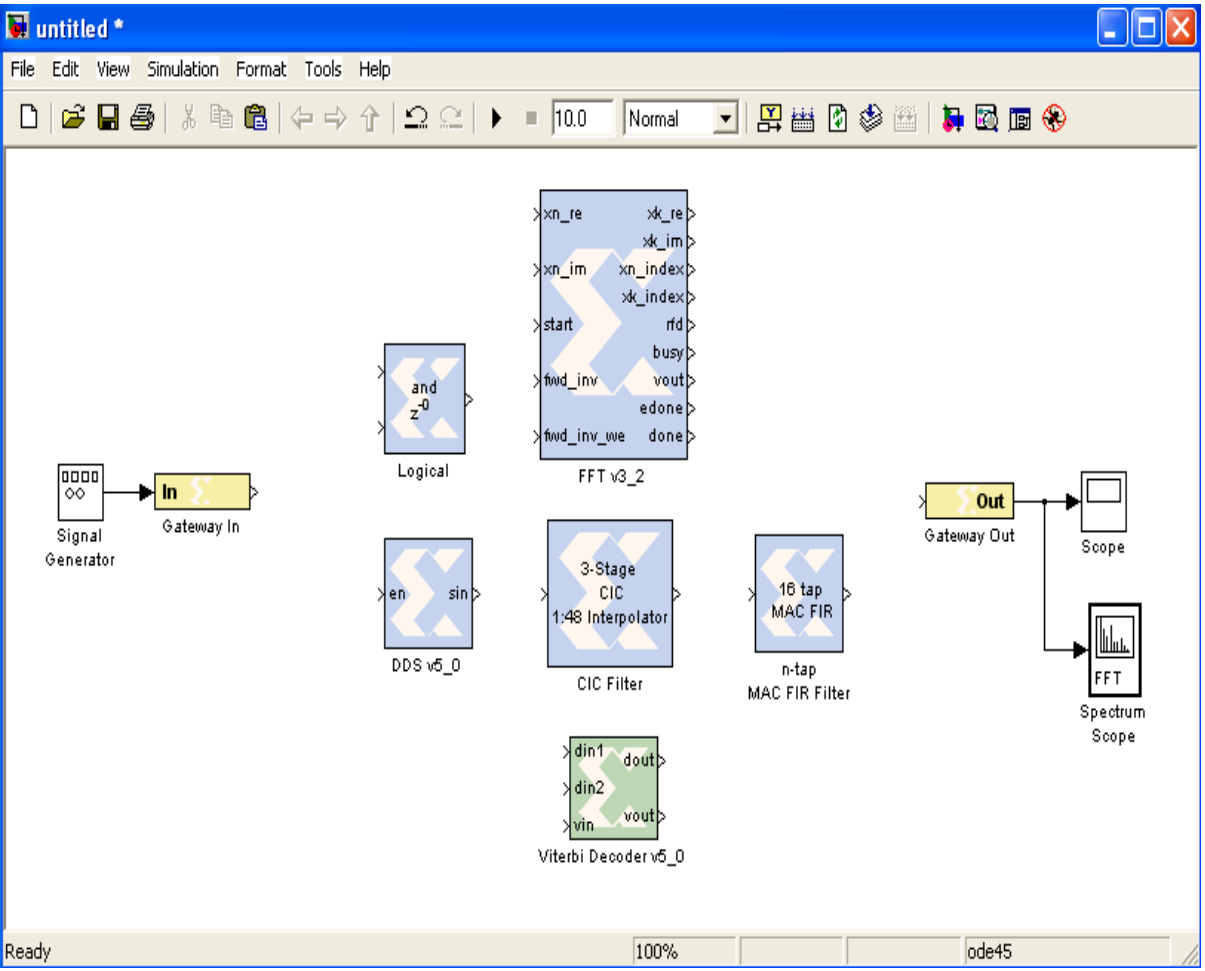
FDA Tool

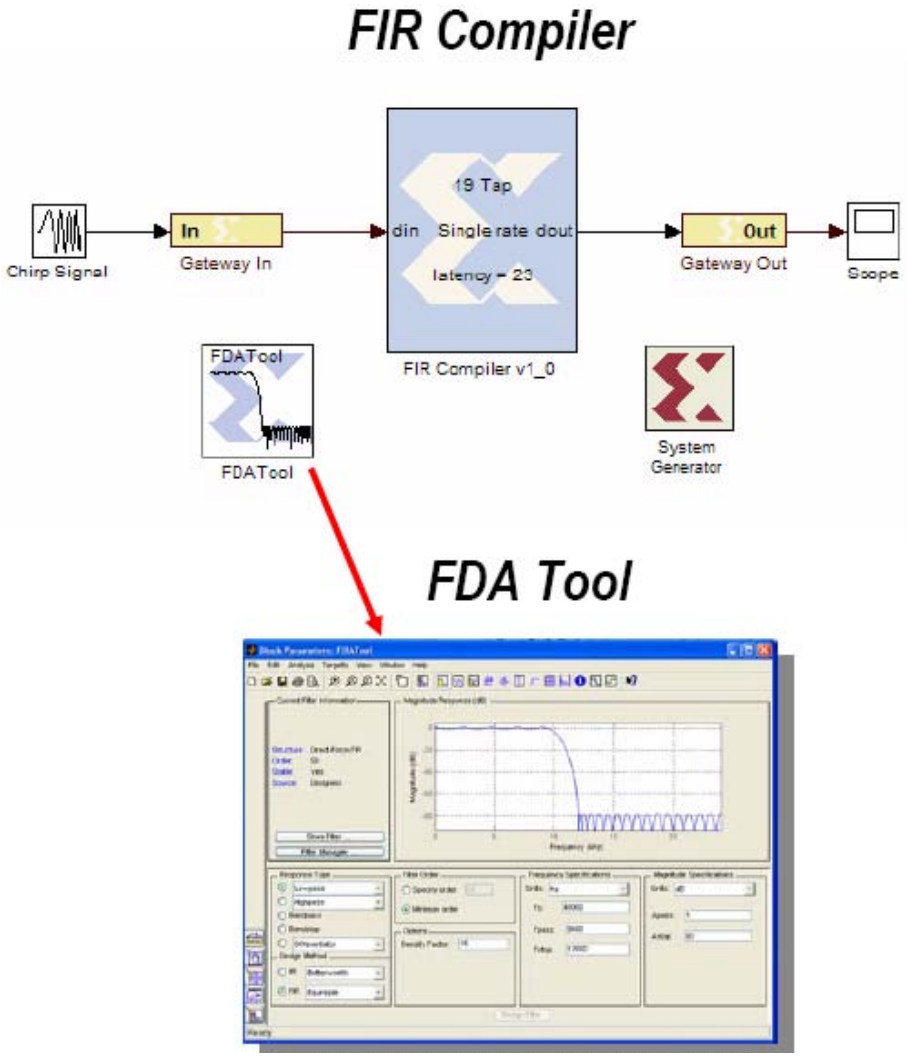


System Modeling in Simulink

Innovative Integration
... real time solutions!

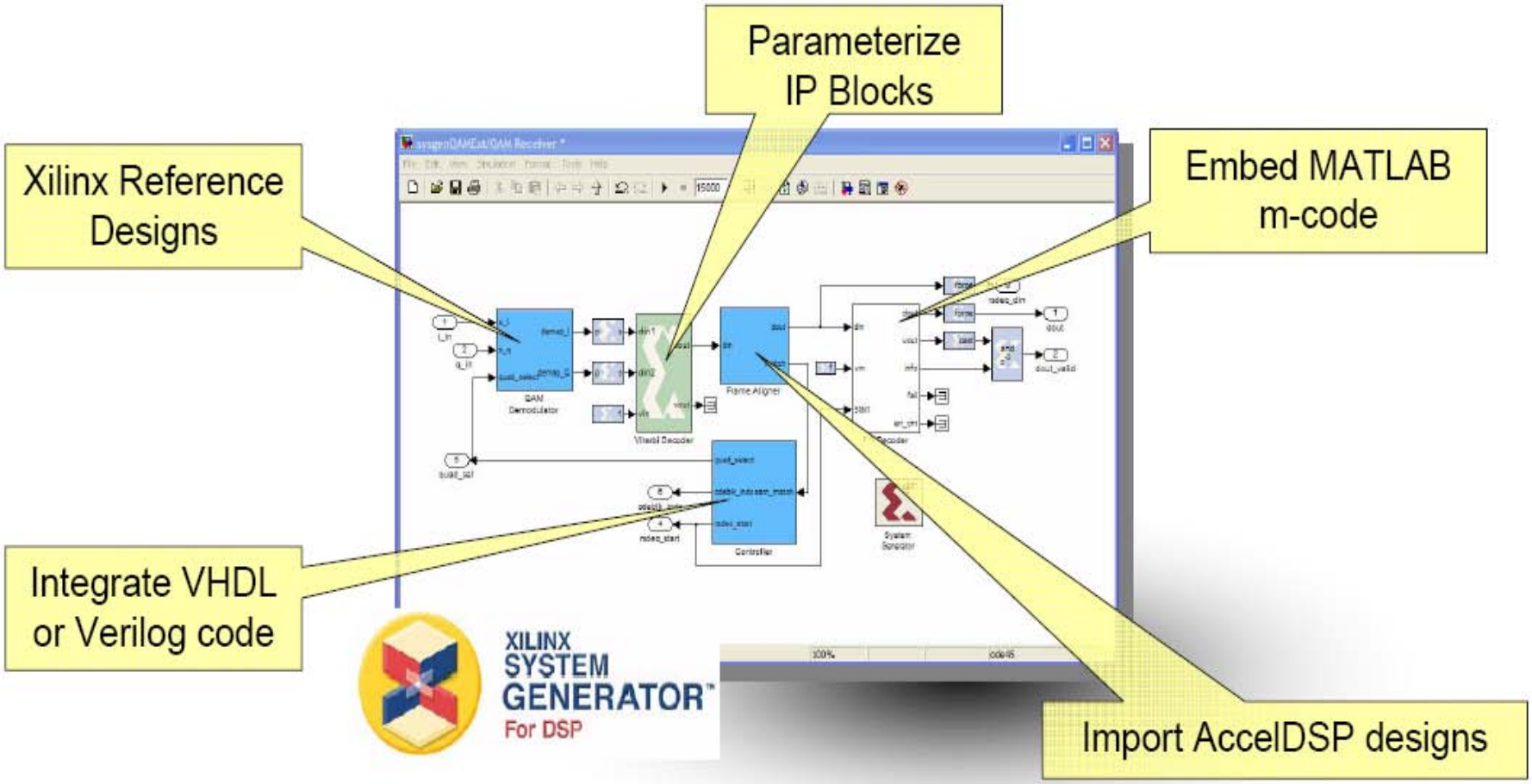
- Visualized debugging tools
- Reliable IP cores
- No multiple clock domain issues





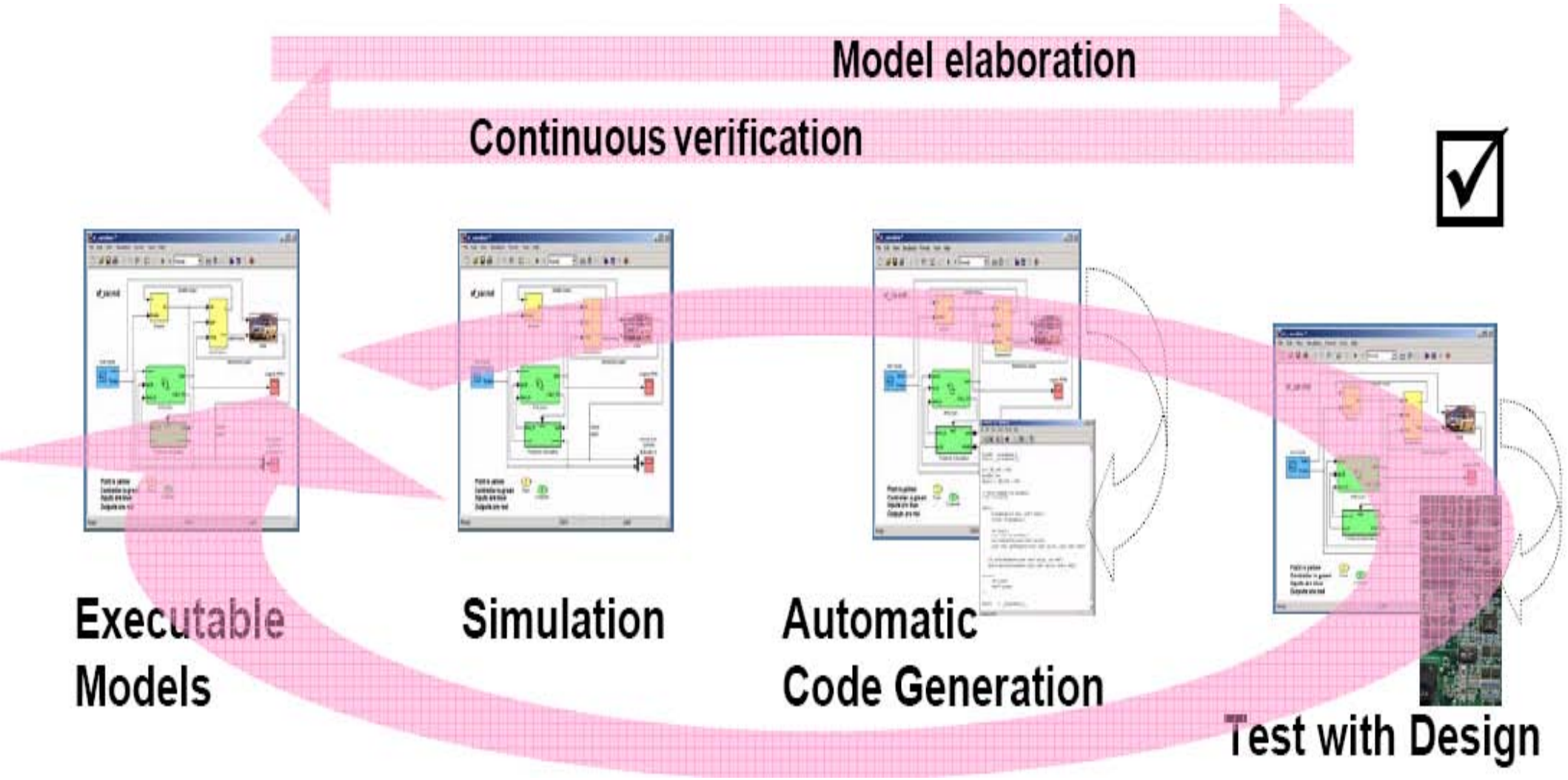
Cores from Various Sources

Innovative Integration
... real time solutions!



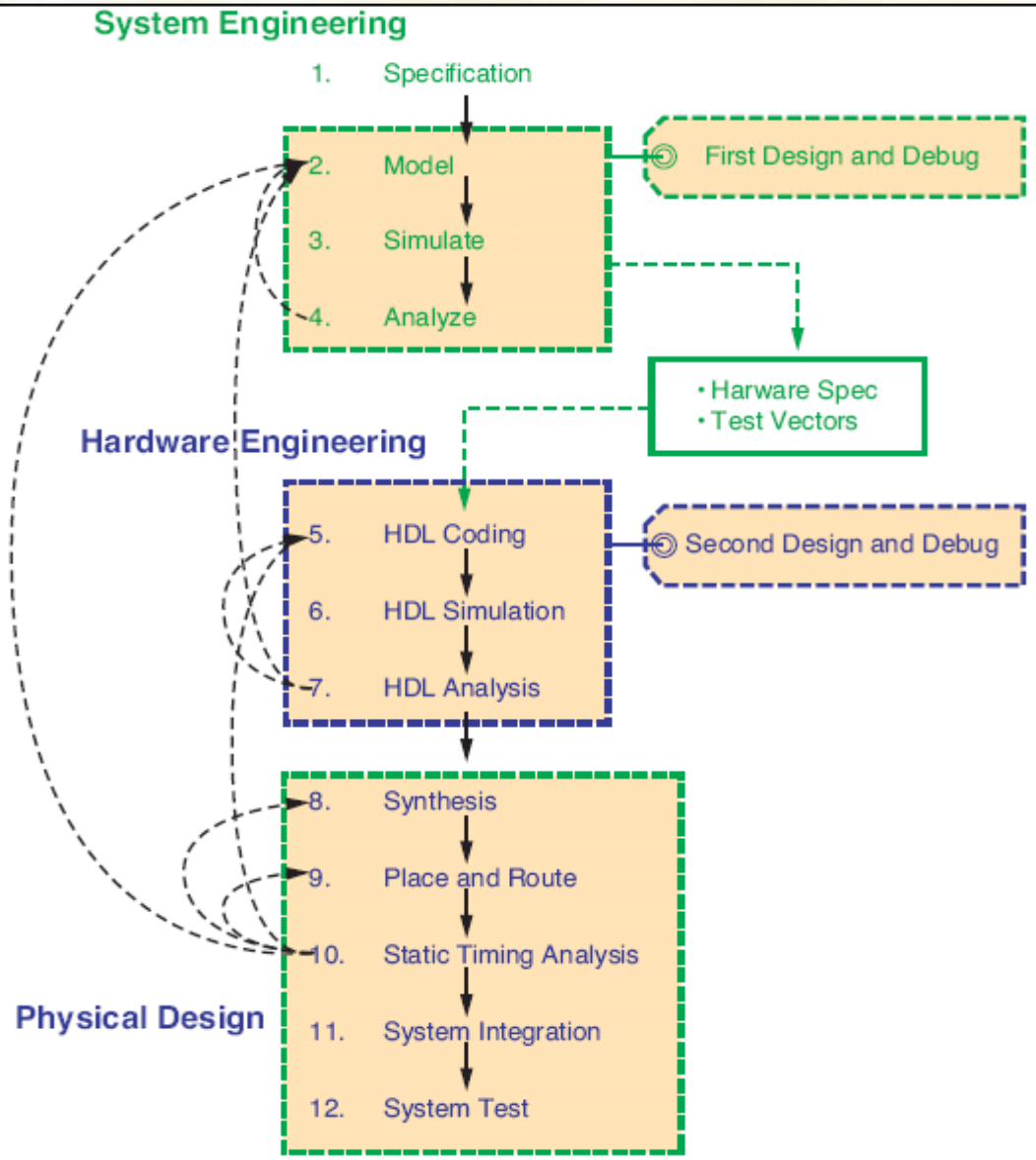
Design Flow in Simulink

Innovative Integration
... real time solutions!



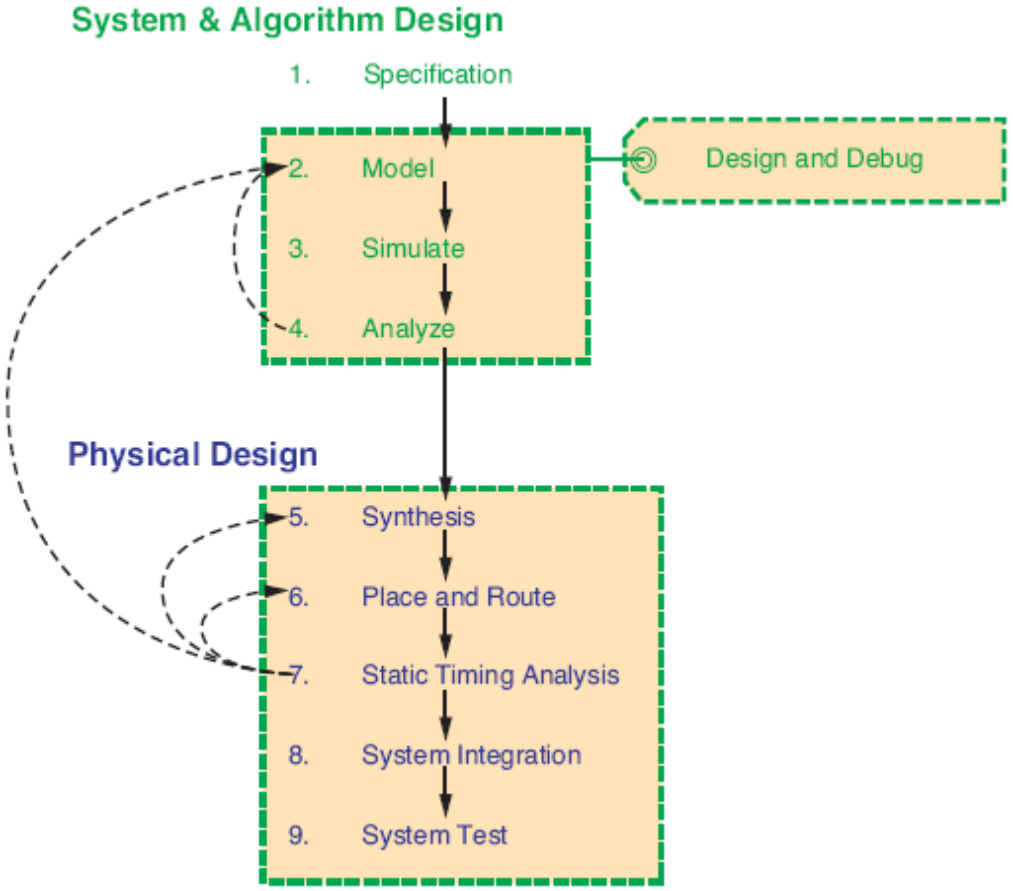
Design Flow Comparison

Innovative Integration
... real time solutions!



Traditional VHDL Coding

- System level design, no hardware engineer needed



Xilinx System Generator

Source: DSP Magazine, May 2006 p.37

II MATLAB BSP

Innovative Integration
... real time solutions!

Advantage

- Save more than 80% time of hand-coding VHDL
  - System Generator : 45.5 hrs
  - Traditional VHDL : 782 hrs
  - Reason: clocking, defect discovery, and component interfaces
- Graphical interfaces for easy project construction
- Visual tools for easy debugging
- Fast simulation ability (Support Modelsim and Chipscope)
- Free

Now support: Quadia, Quixote, PMC UWB, TX, DR, P25M, X3 Family

Source: DSP Magazine, May 2006 p.40

MATLAB BSP Reduces Verification Time

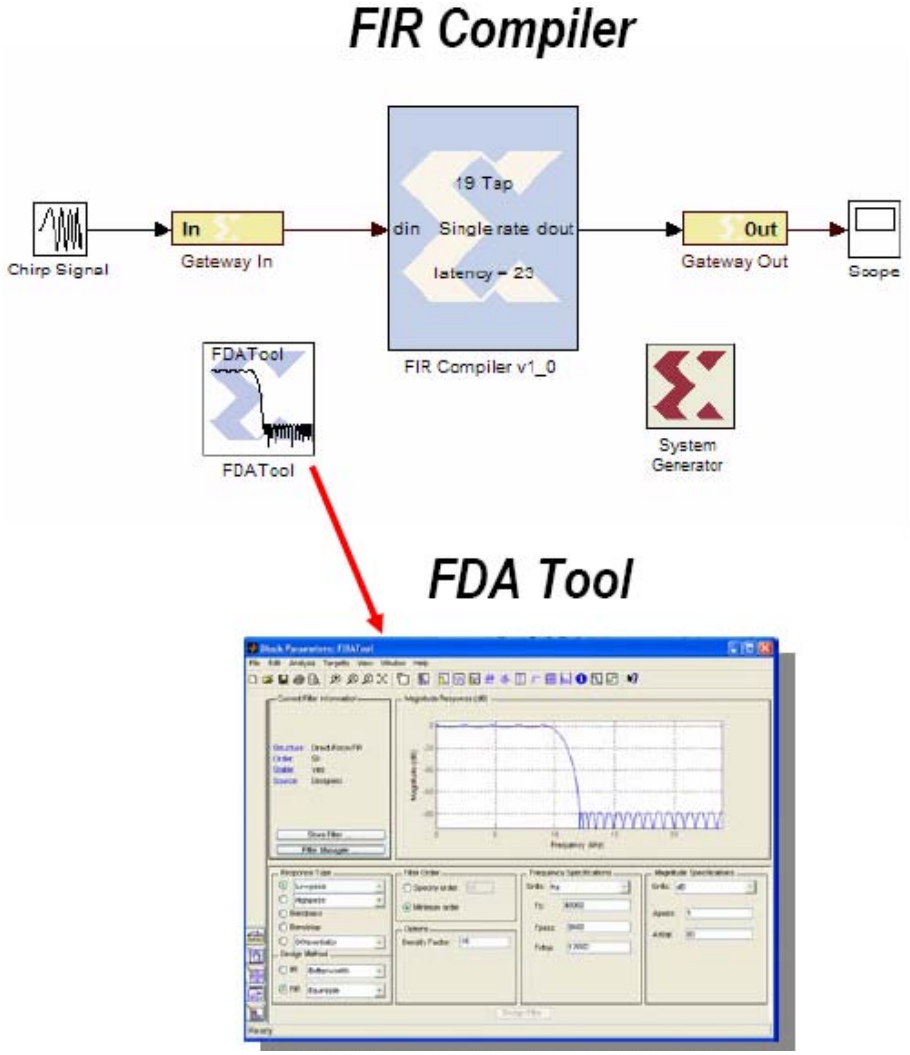
Innovative Integration
... real time solutions!

Design	Simulation Time (Seconds)		
	Software	HW Co-Sim	Increase
Beamformer	113	2.5	45X
OFDM BER Test	742	.75	989X
DUC CFR	731	23	32X
Color Space Converter	277	4	69x
Video Scalar	10422	92	113X

Co-Sim Integrates MATLAB Design Tools with Hardware

Innovative Integration
... real time solutions!

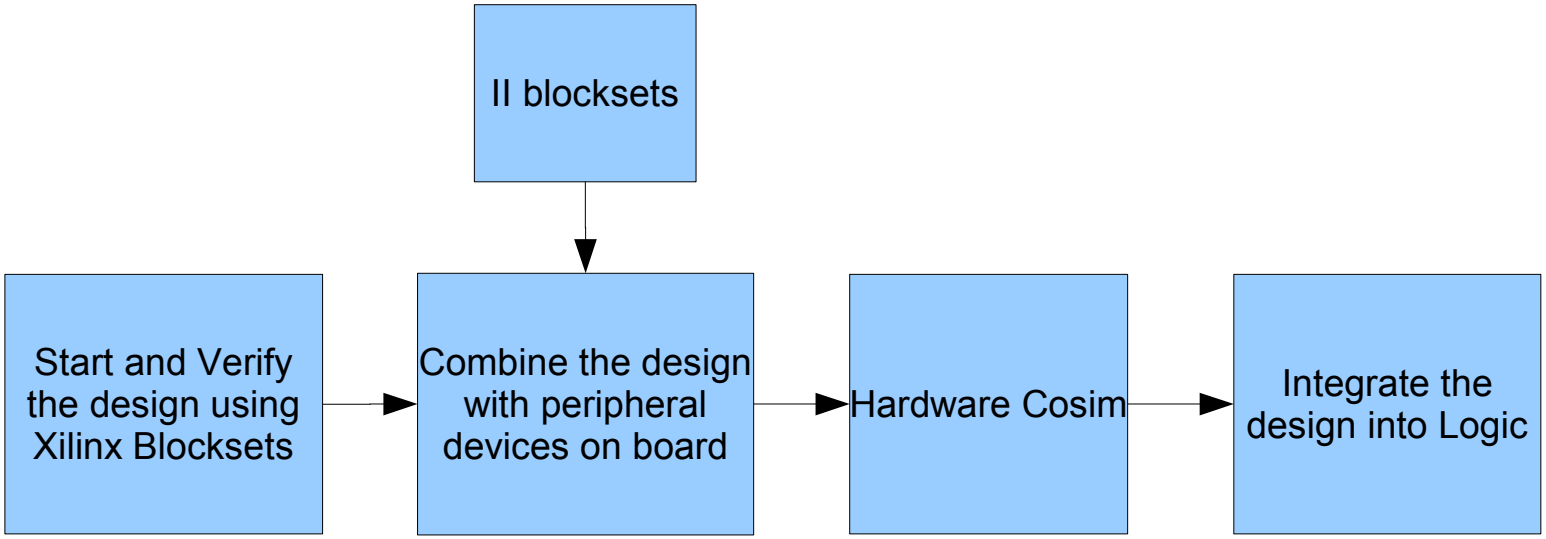
- Access the hardware *DIRECTLY* from MATLAB
- Use powerful MATLAB tools for DSP design and test
- Xilinx System Generator tools link Simulink to the hardware through the BSP
- Hardware Co-simulation radically improves system design and test by reducing design and debug effort



Design Flow

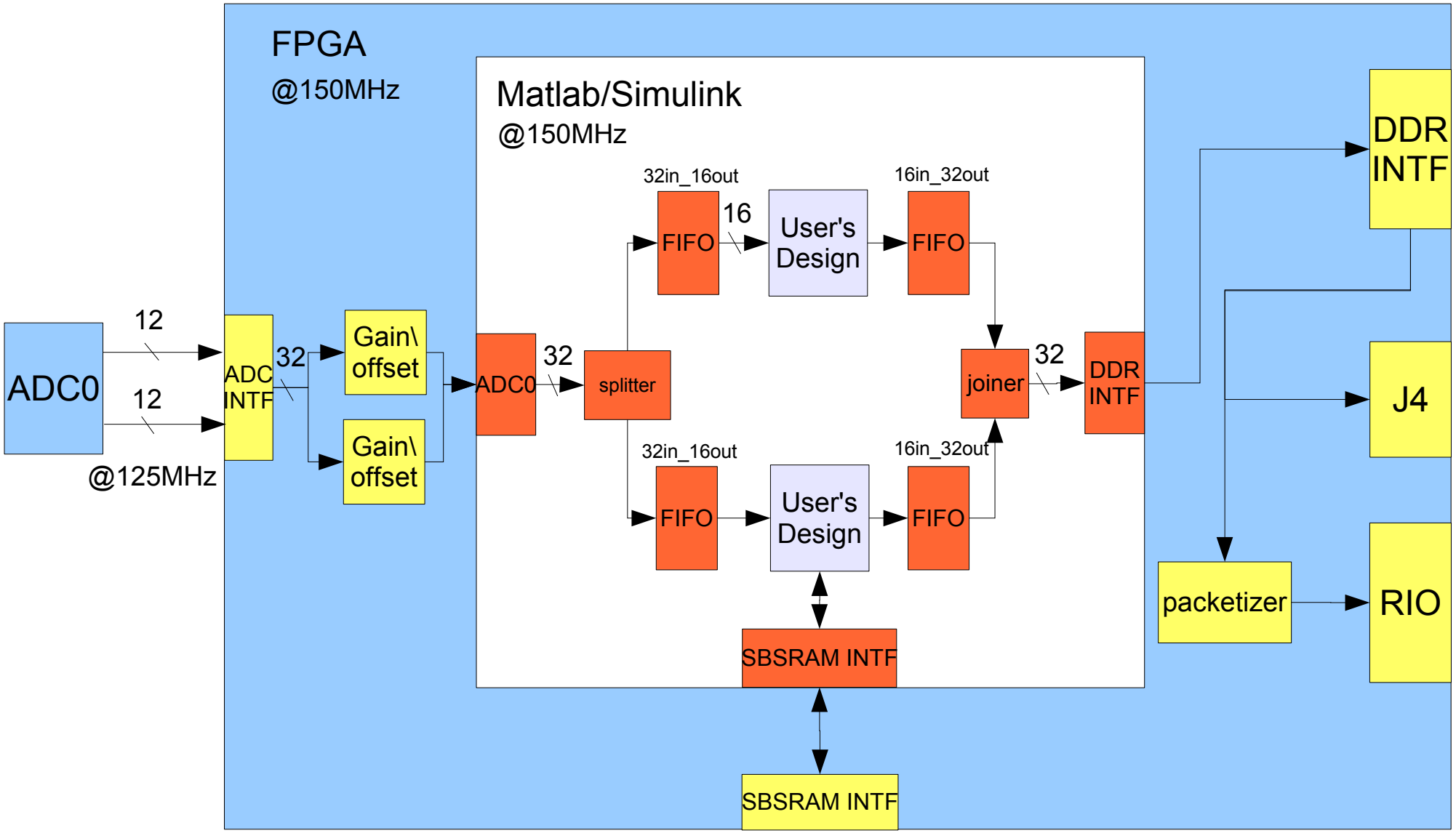
Innovative Integration
... real time solutions!

- Step 1. Start your design in Simulink
- Step 2. Attach II blocks to the design
- Step 3. Hardware co-simulation
- Step 4. Implementation



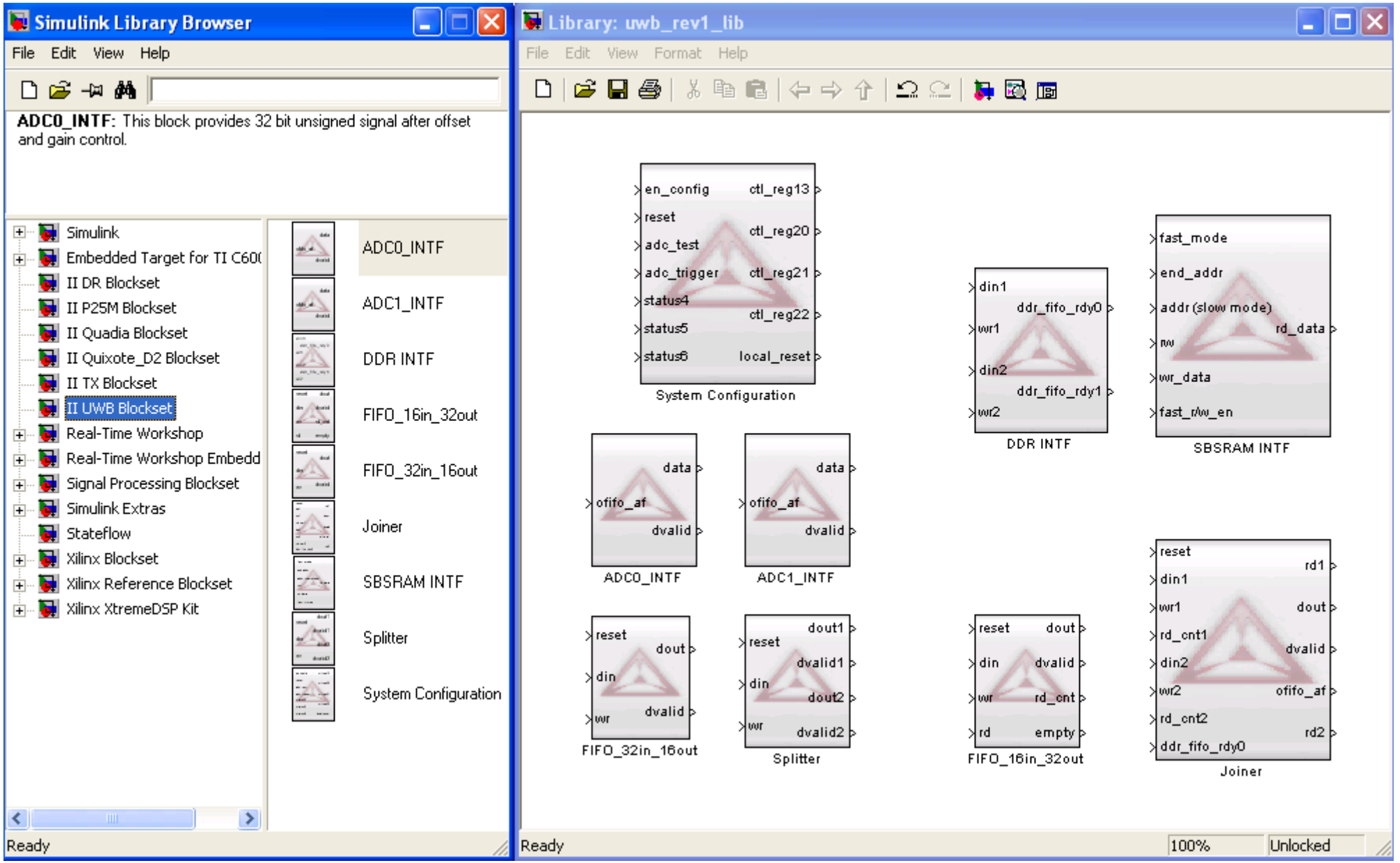
PMC UWB Block Diagram

Innovative Integration
... real time solutions!



II PMC UWB Library

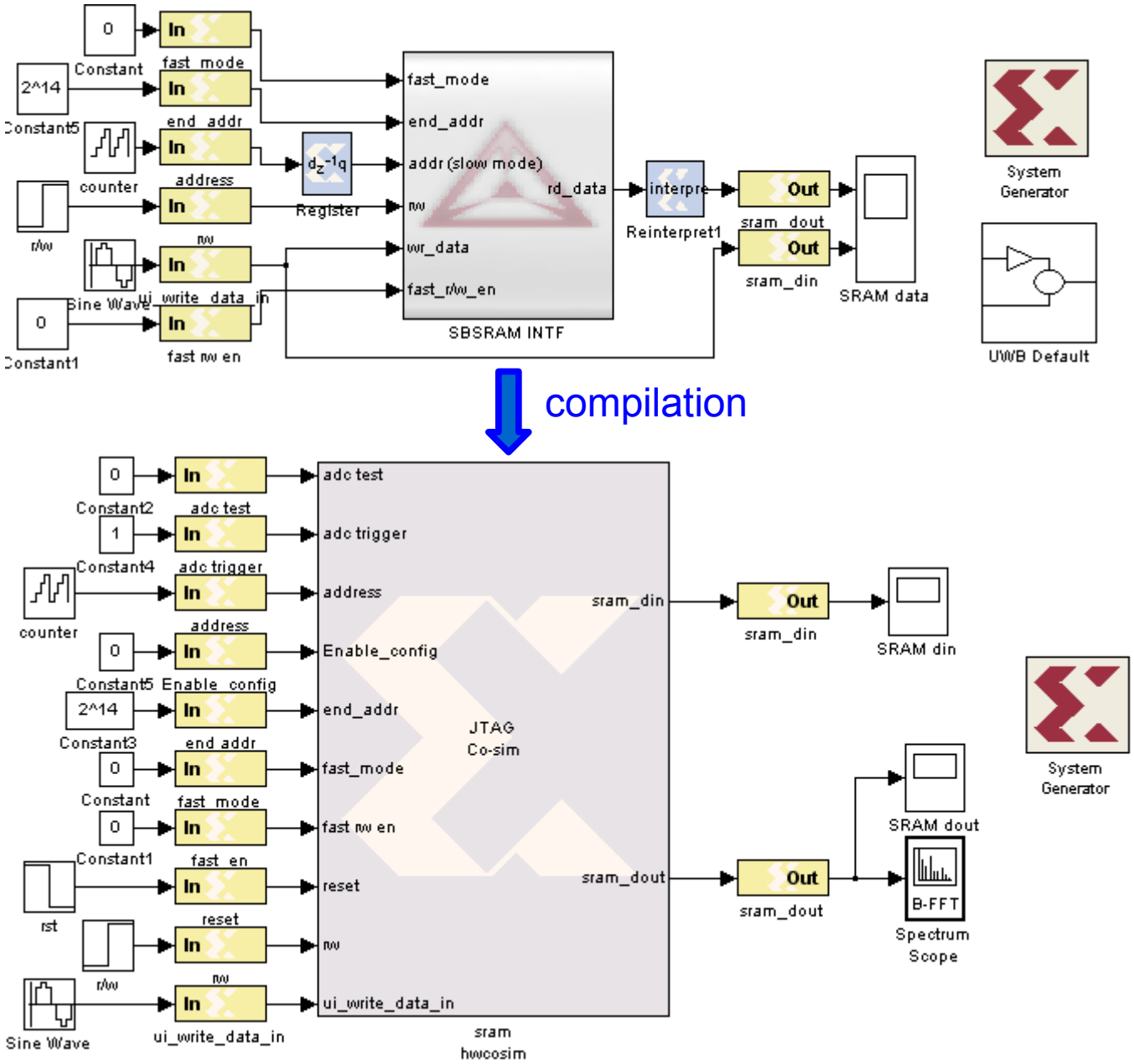
Innovative Integration
... real time solutions!



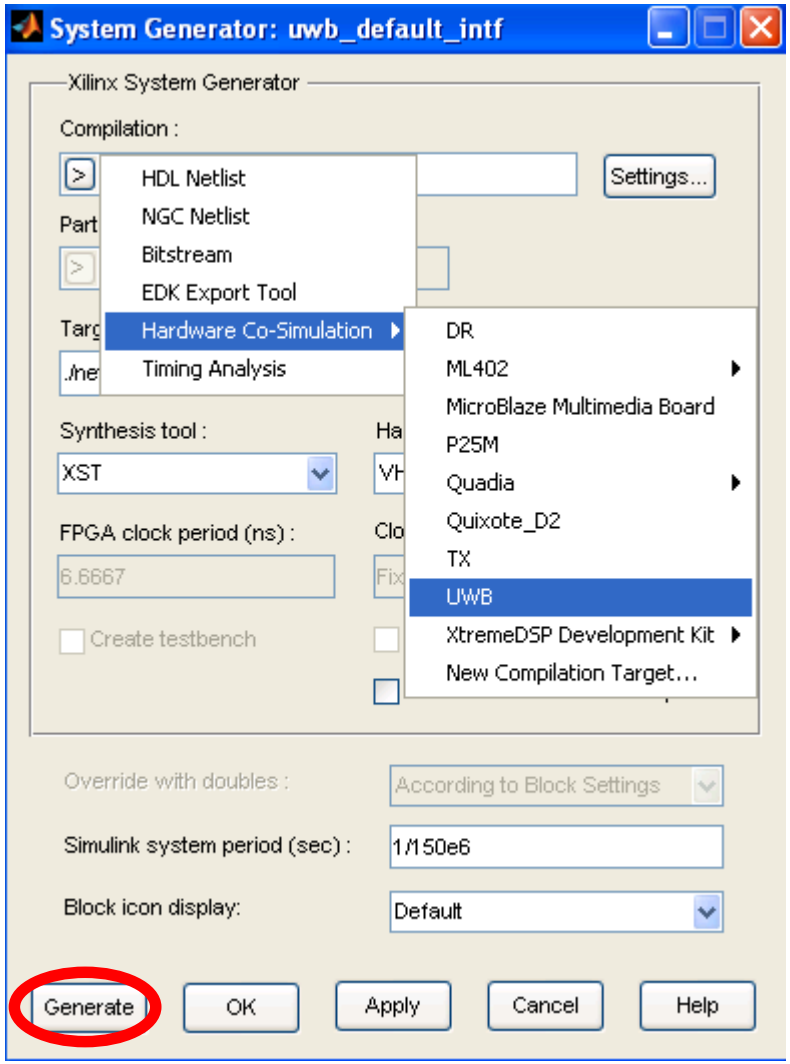
Hardware Co-simulation

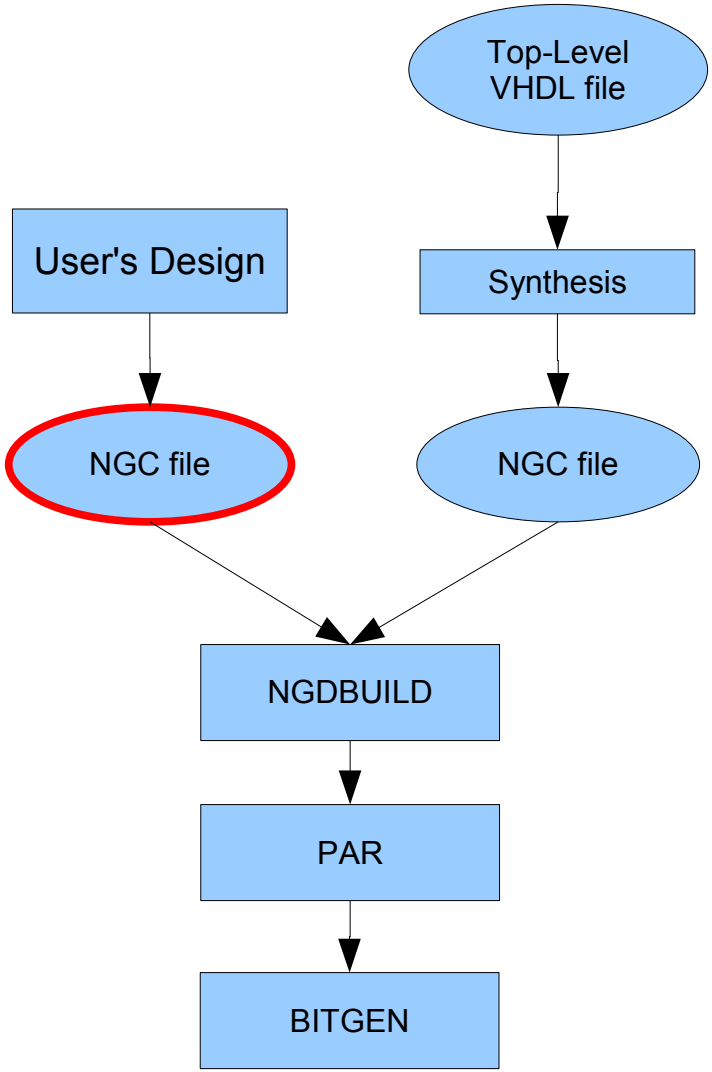
Innovative Integration
... real time solutions!

- Bit true, cycle true, hardware-in-the-loop simulation
- Fast simulation with infrastructures on the board



Compilation Flow

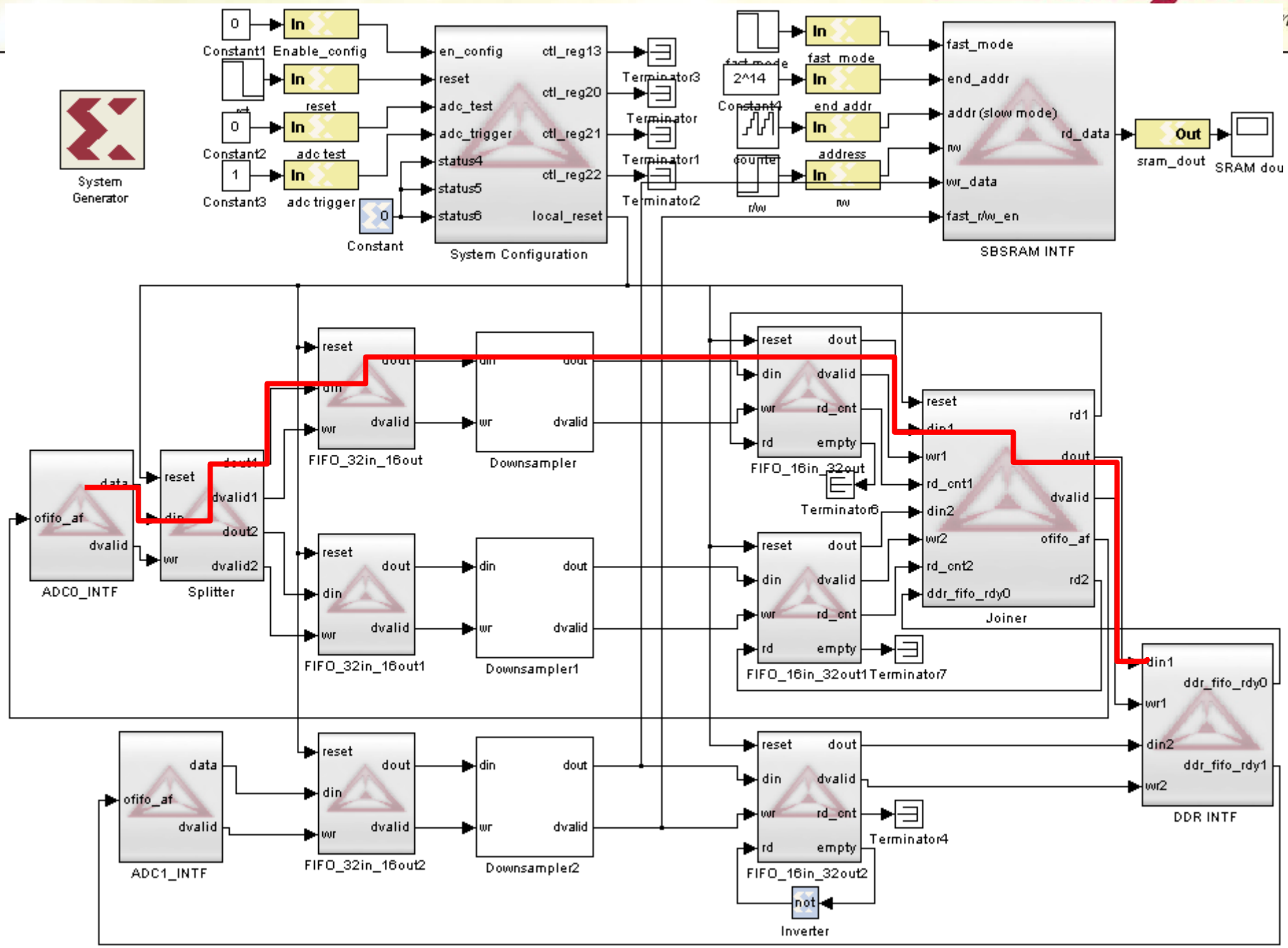




Demo

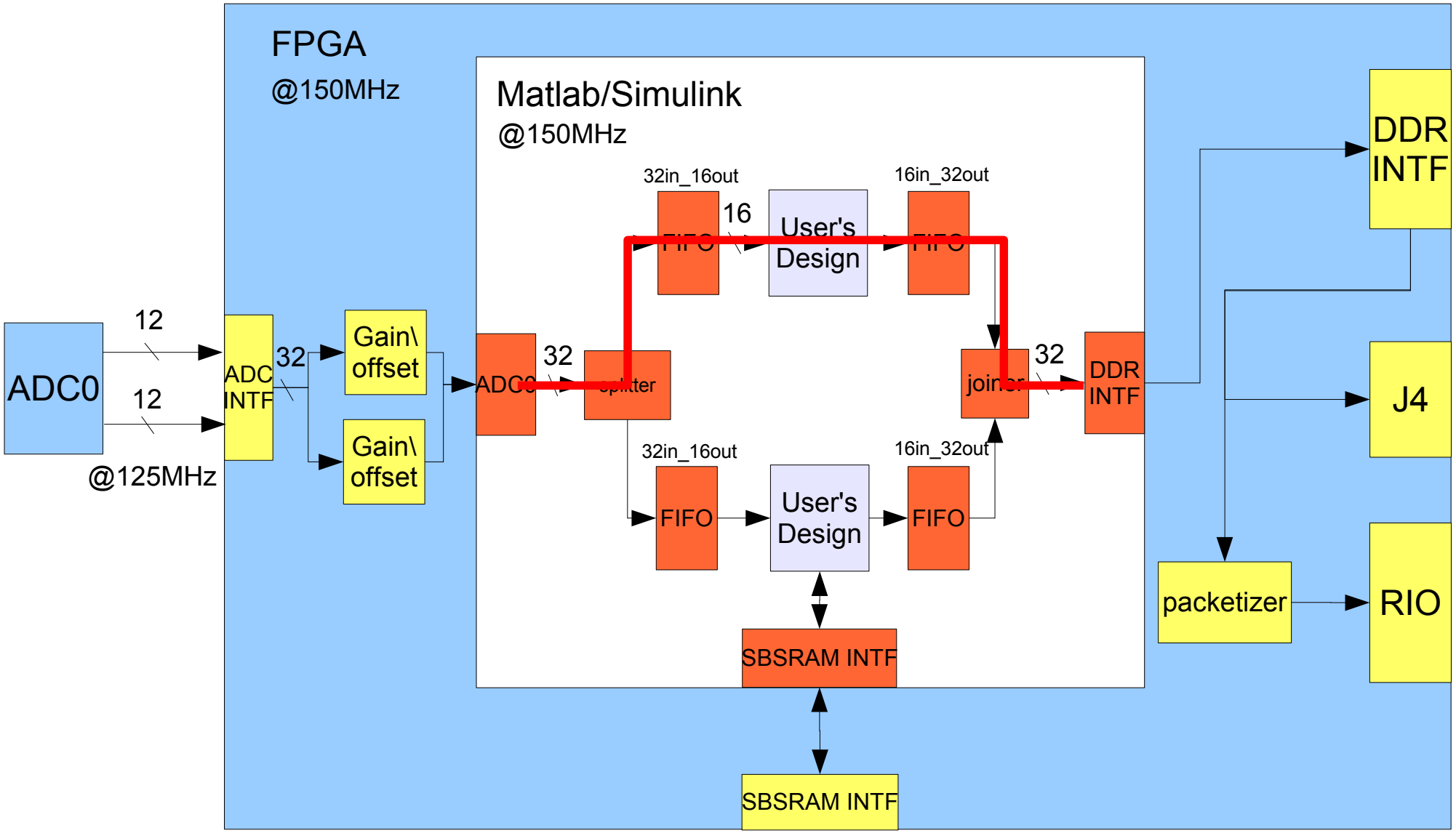
Build Your Design

Innovative Integration



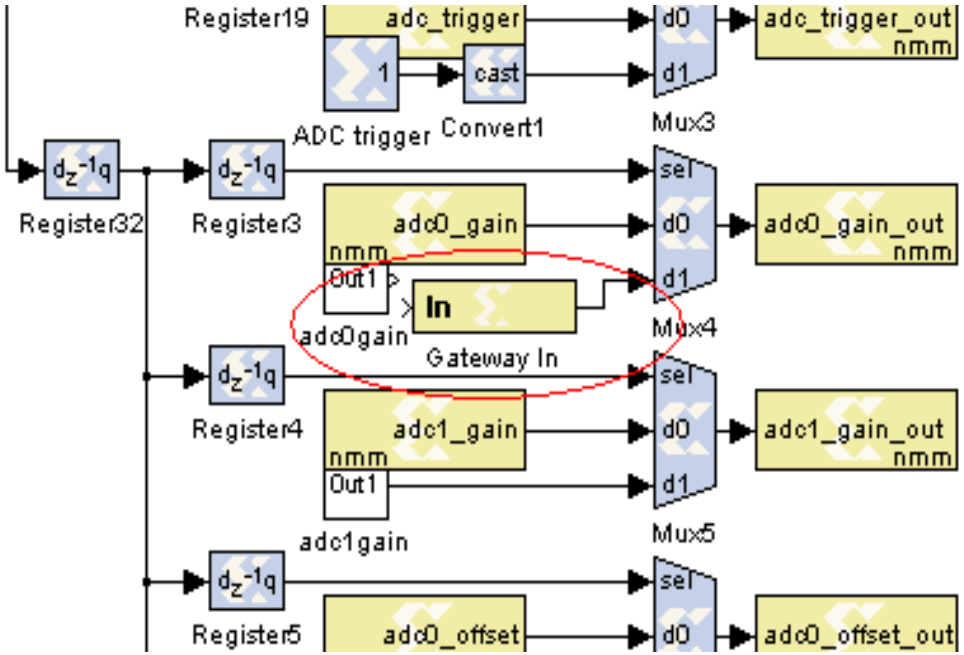
PMC UWB Block Diagram

Innovative Integration
... real time solutions!



NEW Feature – System Configuration Panel

- Easy configuration
- No software needed
- Capability of changing settings on the fly



Innovative

Function Block Parameters: System Configuration

UWB Simulink Block (mask)

This block sets up the command registers in Matlab. When "Enable Configuration" is '1', all prameters are provided by Matlab. When "Enable Configuration" is '0', the parameters are from the host. Four 32 bit host controlled registers 13, 20, 21, and 22 can be monitored inside Matlab. Three 32 bit status ports provide information of user's design to the host. Please refer to Registers section in FrameWork Logic User Guide for more information.

Parameters

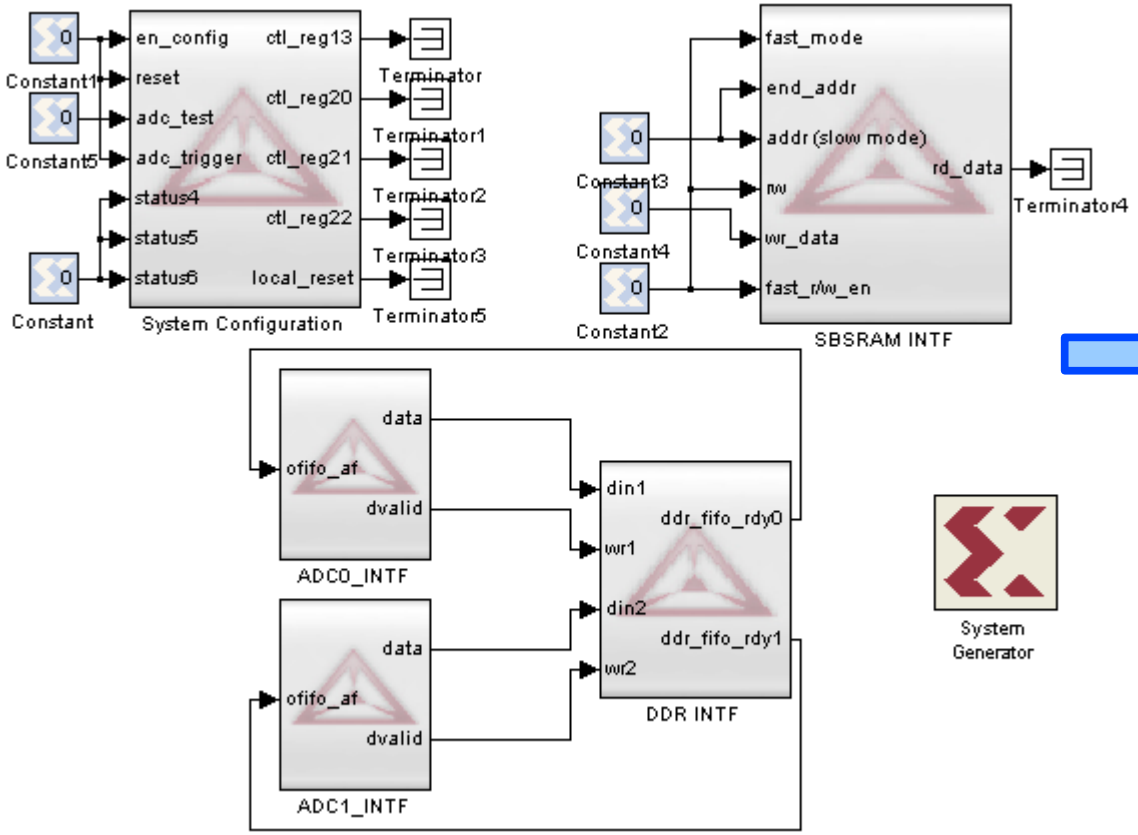
- [x] Run
- [x] ADC0 Channel Enable
- ADC0 Clock Select: PLL
- ADC0 Desitinations: PCI
- ADC0 Gain (0 - 2): 1
- ADC0 Offset (2^0 - 2^15): 0
- [x] ADC1 Channel Enable
- ADC1 Clock Select: PLL
- ADC1 Desitinations: PCI
- ADC1 Gain (0 - 2): 1
- ADC1 Offset (2^0 - 2^15): 0
- [ ] Bypass VCO
- Xtal Sel: Xtal
- PLL Feedback Divider Ratio M (1 - 512): 28
- PLL Output Divider Ratio N: N=4
- Sync Clock Select: ACLK
- Divider Clock Select: ACLK
- Divider Ratio: D=1

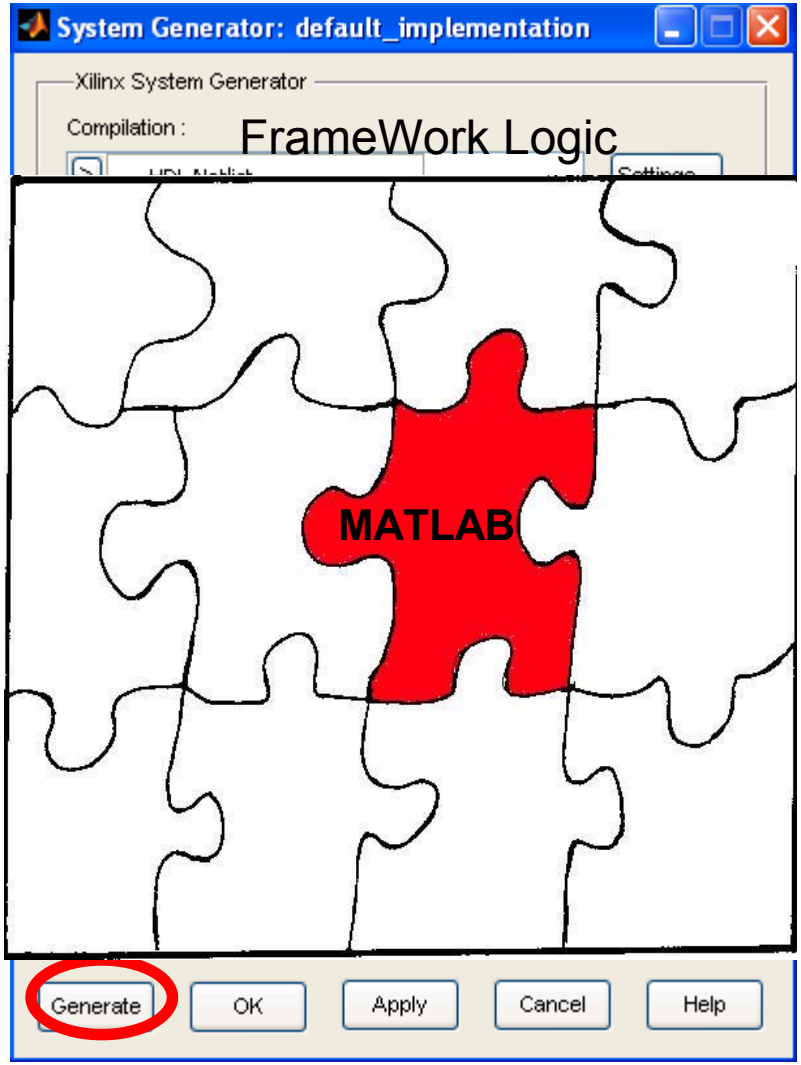
OK | Cancel | Help | Apply

Integrating MATLAB Core into FrameWork Logic

Innovative Integration
... real time solutions!

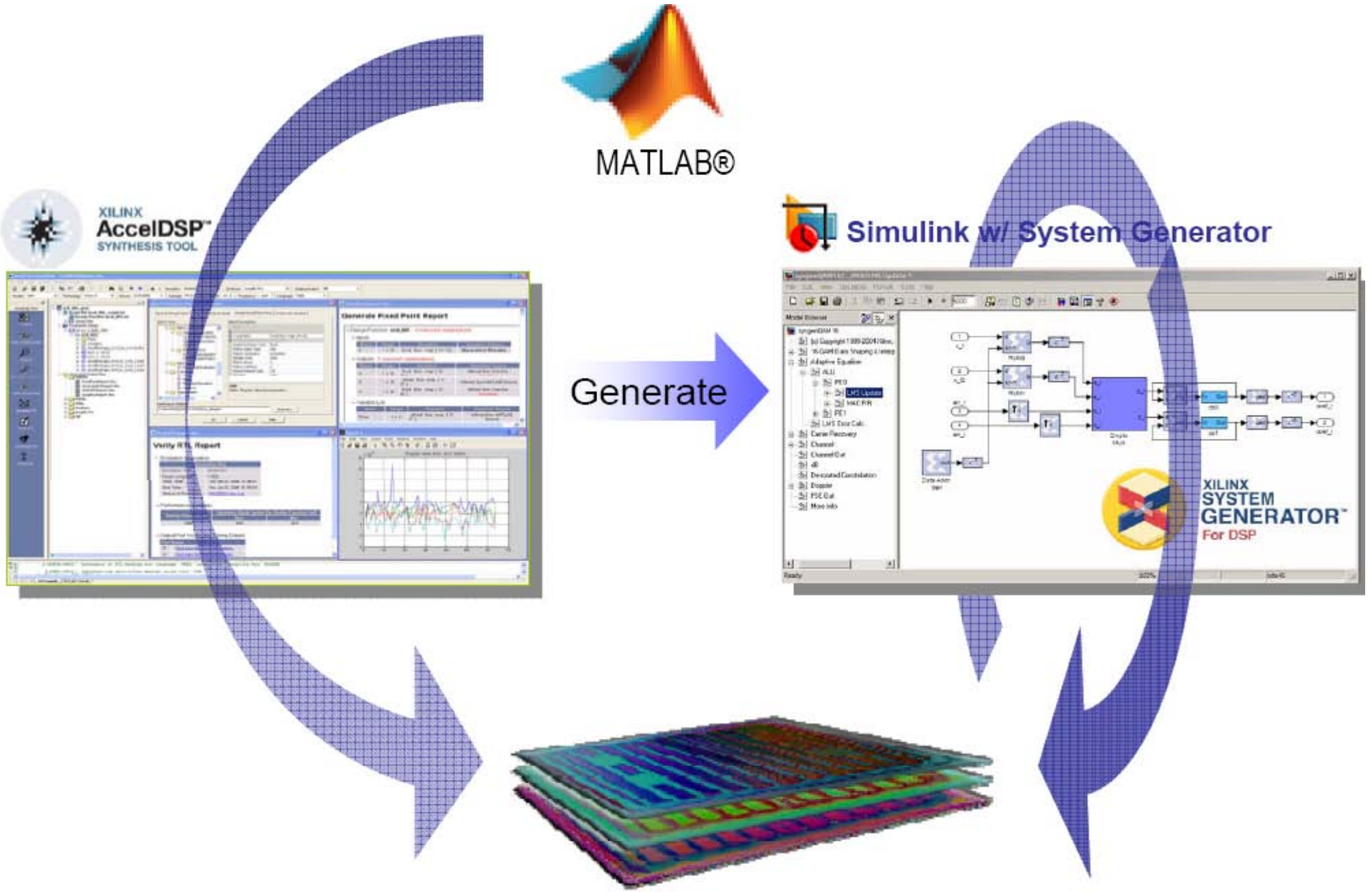
Replace Gateways with constants for final implementation





Design in MATLAB/Simulink

Innovative Integration
... real time solutions!



FrameWork VHDL Logic Design

II FrameWork Logic

Innovative Integration
... real time solutions!

- Framework Logic Features
  - Comprehensive board support packages in MATLAB and VHDL for FPGA signal processing development
  - Hardware interface layer design structure allows rapid integration of application specific code
  - Designed to support real time signal processing and data acquisition
- Complete end-to-end simulation testbench using ModelSim
- Reference designs illustrating hardware use
  - Saves time by providing a simplified access to the hardware and data stream
  - Supported by software for control, data logging and signal generation
  - Get you off to a quick start

→ *Reduced design, test and verification time*

Innovative IP Core Library

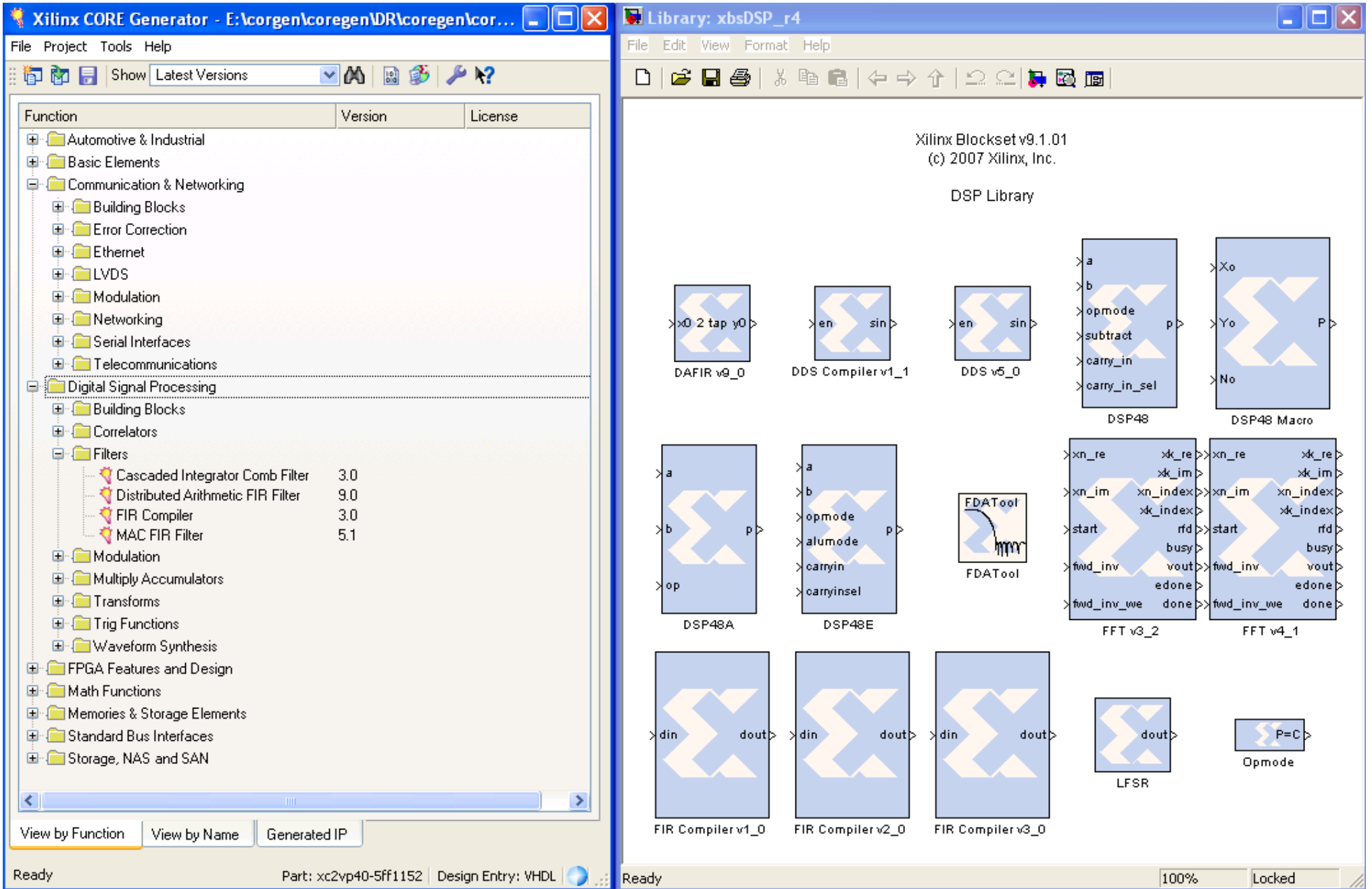
Innovative Integration
... real time solutions!

Hardware Control Cores	Function
Virtual FIFO	Implements a FIFO using DDR DRAM memory buffer
Multi-queue FIFO	Implements multiple FIFO queues in DDR DRAM memory buffer
Pattern Generator	Implements a dynamically loadable pattern generator for DDR DRAM capable of >500 MB/s sustained operation
SRAM Controller	Provides high speed synchronous SRAM interface
Packetizer	Packetizes data for system interfaces
Deframer	Unpacketizes data from system interface
J4 Link	Implements a data link over PMC J4 connection to base cards capable of >350 MB/s
SFP Data link	Provides an SFP data link interface (Quadia)
RIO Data Link	Provides a RIO link interface between FPGAs with flow control
DSP interfaces	Interface cores for standard TI DSPs ('6416, '6713)
DDC Interface	Interface to TI GC5016 quad-channel DDC devices
Quadrature Decoding	Interface to industry-standard quadrature encoders
Sigma Delta DAC	Sigma Delta modulator and controls implements a DAC function. External analog filter is required.
Triggering Controls	Snapshots, external triggering, decimation

DSP Cores	Function
Digital Downconversion	20 channels DDC operating at up to 208 MHz
Spectral Inverter	Real-time spectral inversion
FFT	Radix-2 FFT, 32 to 8K record lengths
FIR Filters	Support via Xilinx Corelib and Matlab. The number of taps that may be implement for real time operation depends on sample rate, logic utilization and logic clock rate.
CIC Filters	Support via Xilinx Corelib and Matlab.

Xilinx IP Cores

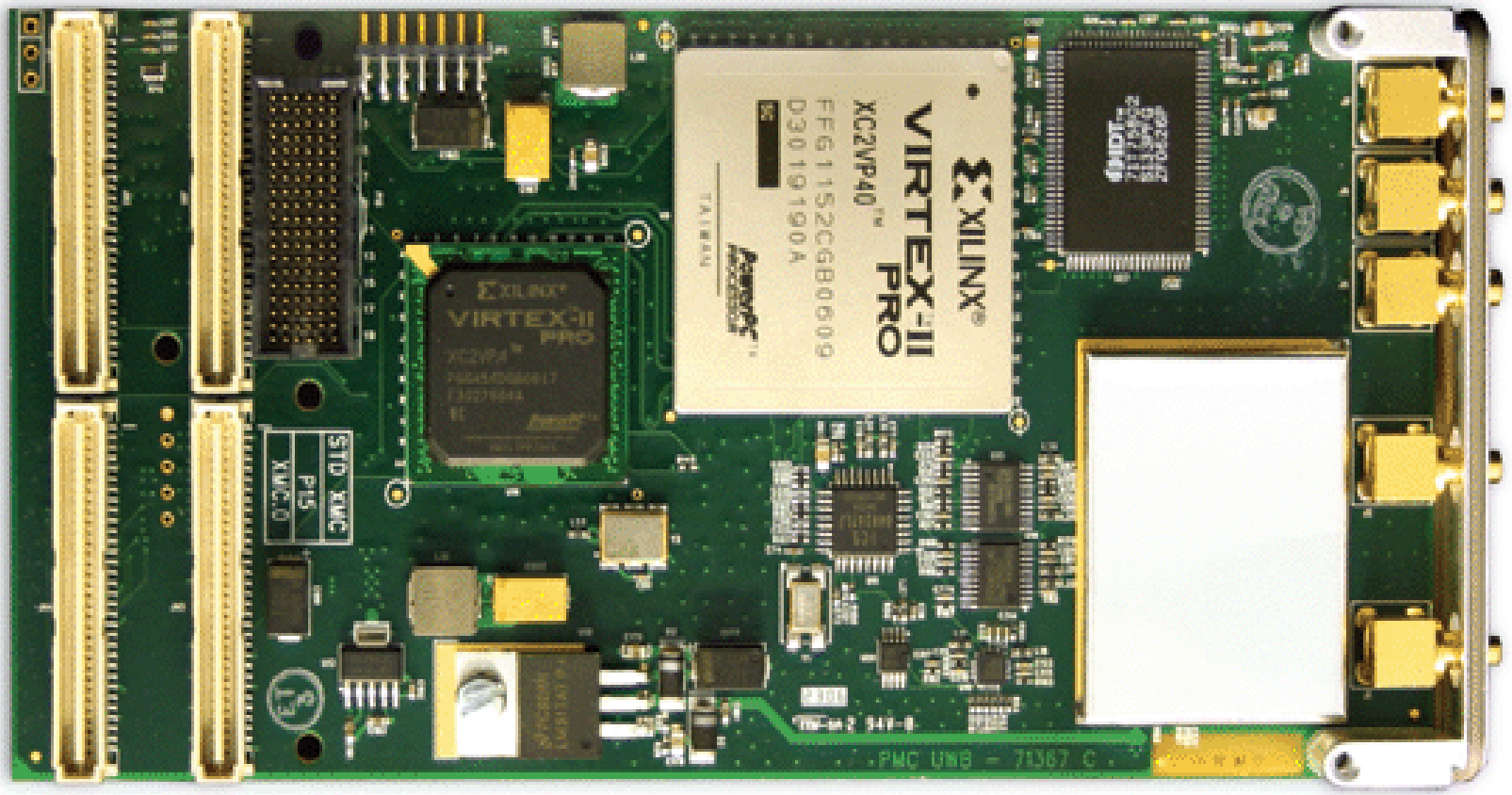
Innovative Integration
... real time solutions!



Example: FIR Filter in UWB

Innovative Integration
... real time solutions!

- Two 12-bit 250 MSPS AD converters
- Virtex-II Pro FPGA, 4 Million gates
- 64MB SDRAM plus 2MB SRAM for FPGA
- Sample clocks: dual external or on-board PLL
- Software Defined Radio (SDR)
- Electronic Warfare
- Advanced RADAR
- Telecom IP development

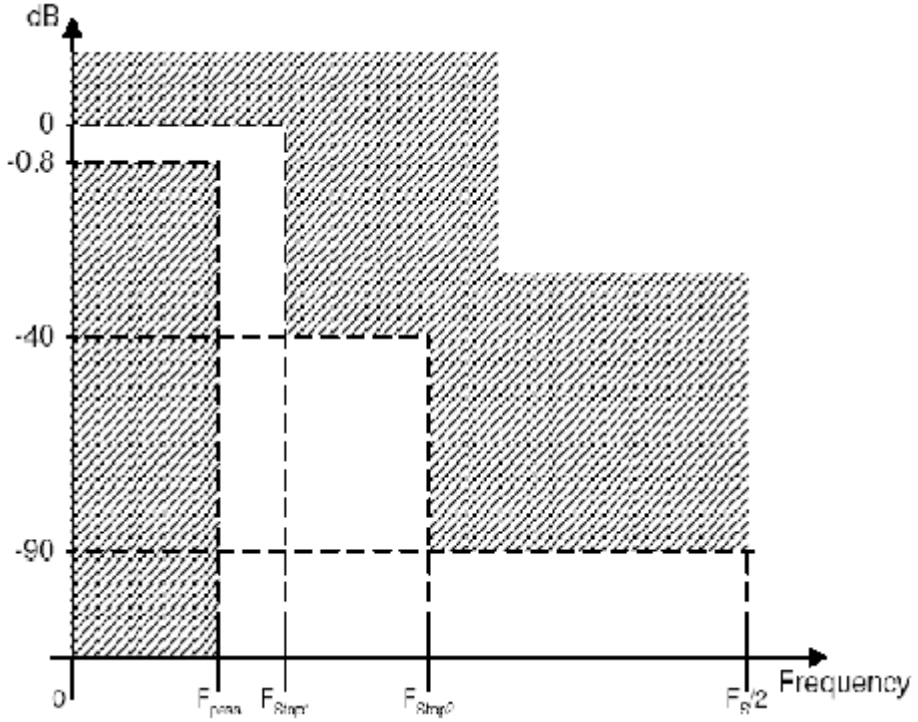


VHDL Design Flow

Innovative Integration
... real time solutions!

Step 1 : Define system requirements and architecture

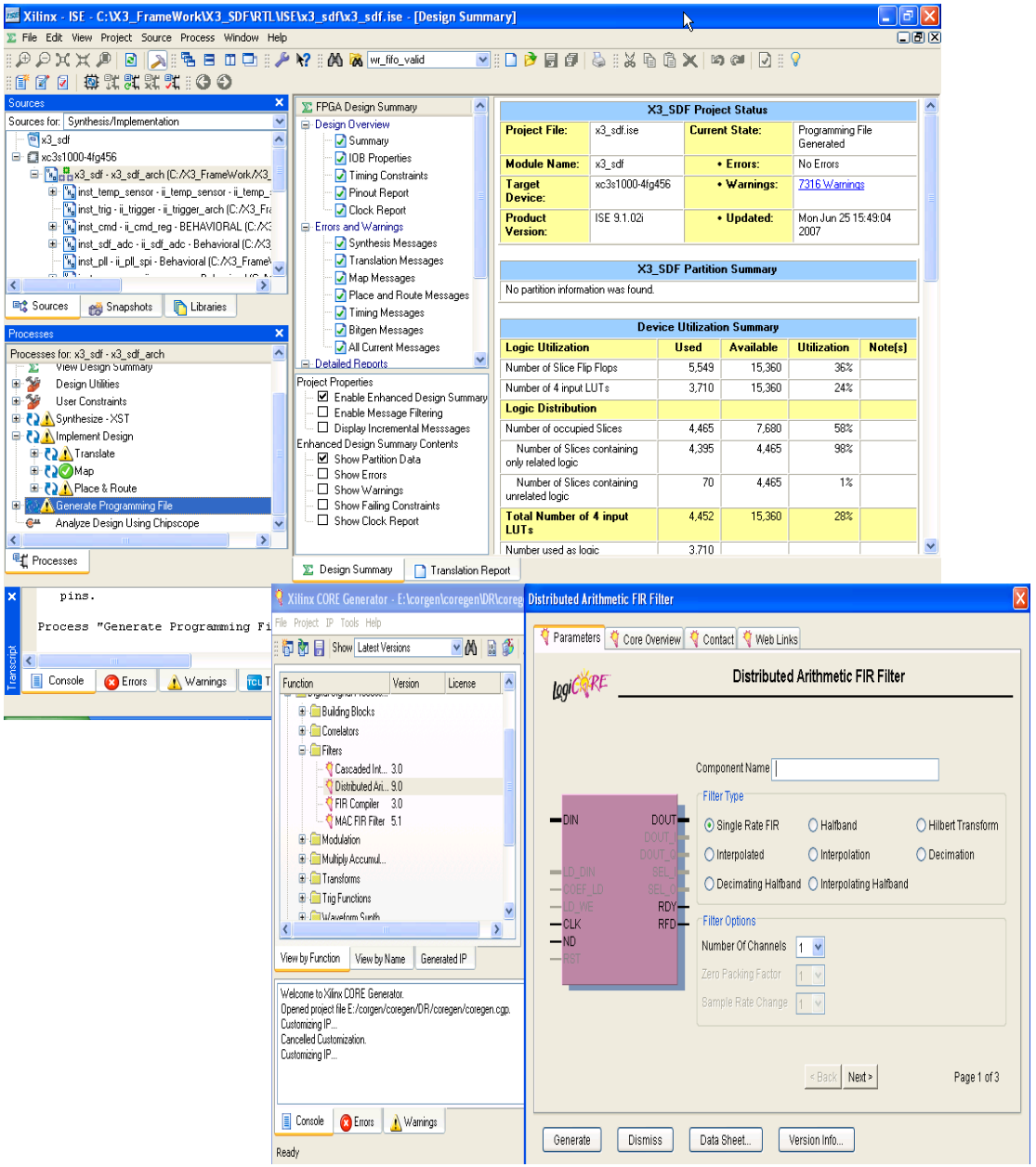
- Define DSP, data analysis, triggering and system control functions
- Define accuracy and dynamic range requirements
- Identify real-time constraints such as data rates and processing rates
- Identify system data buffering requirements
- Estimate logic usage



Step 2 – Create cores and logic

Innovative Integration
... real time solutions!

- Create new logic and cores using Xilinx Core Generator, MATLB, or VHDL
- Simulate and verify core functionality



Step 3 – Add functions to FrameWork Logic

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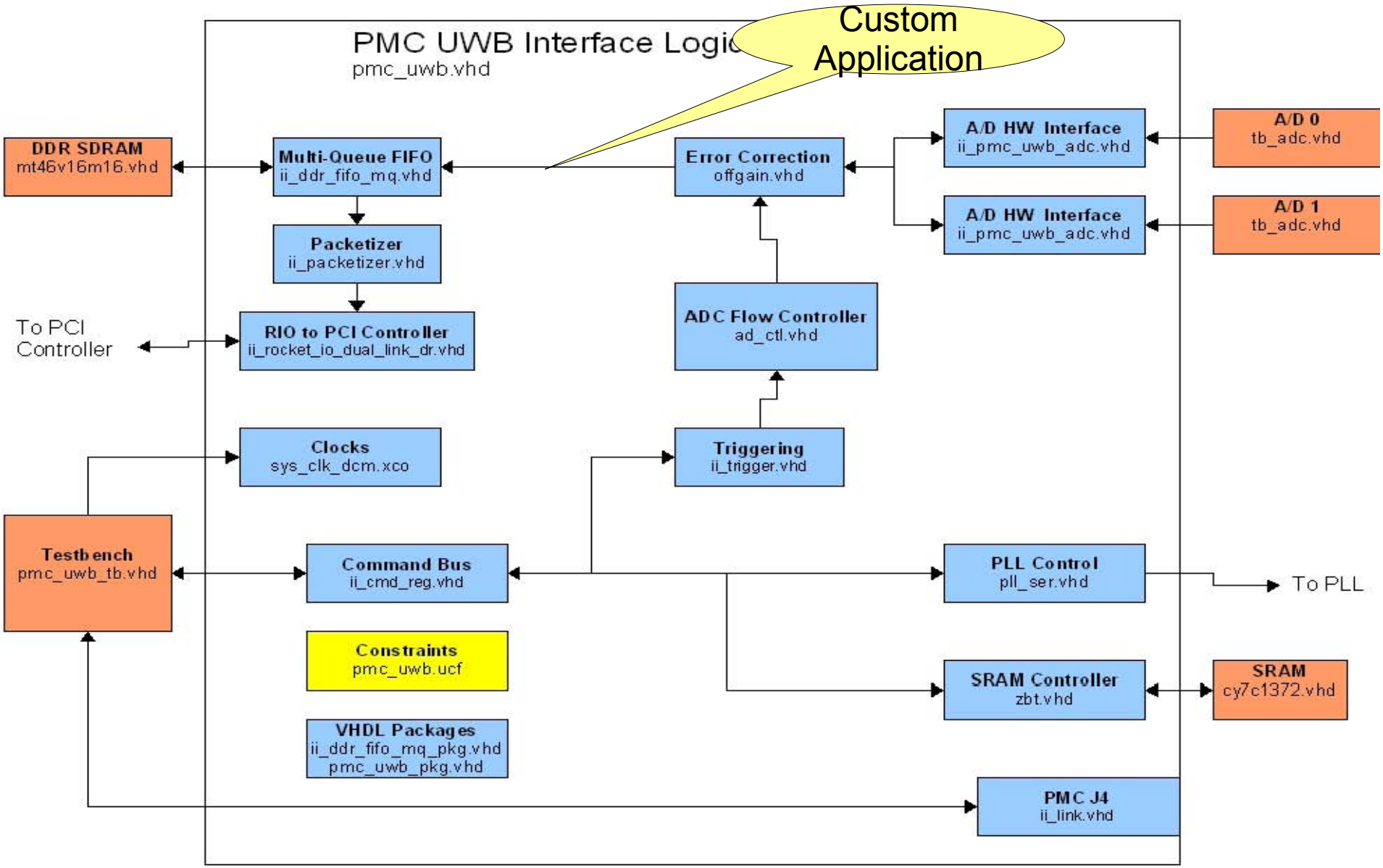
... real time solutions!



Step 4 - Simulation

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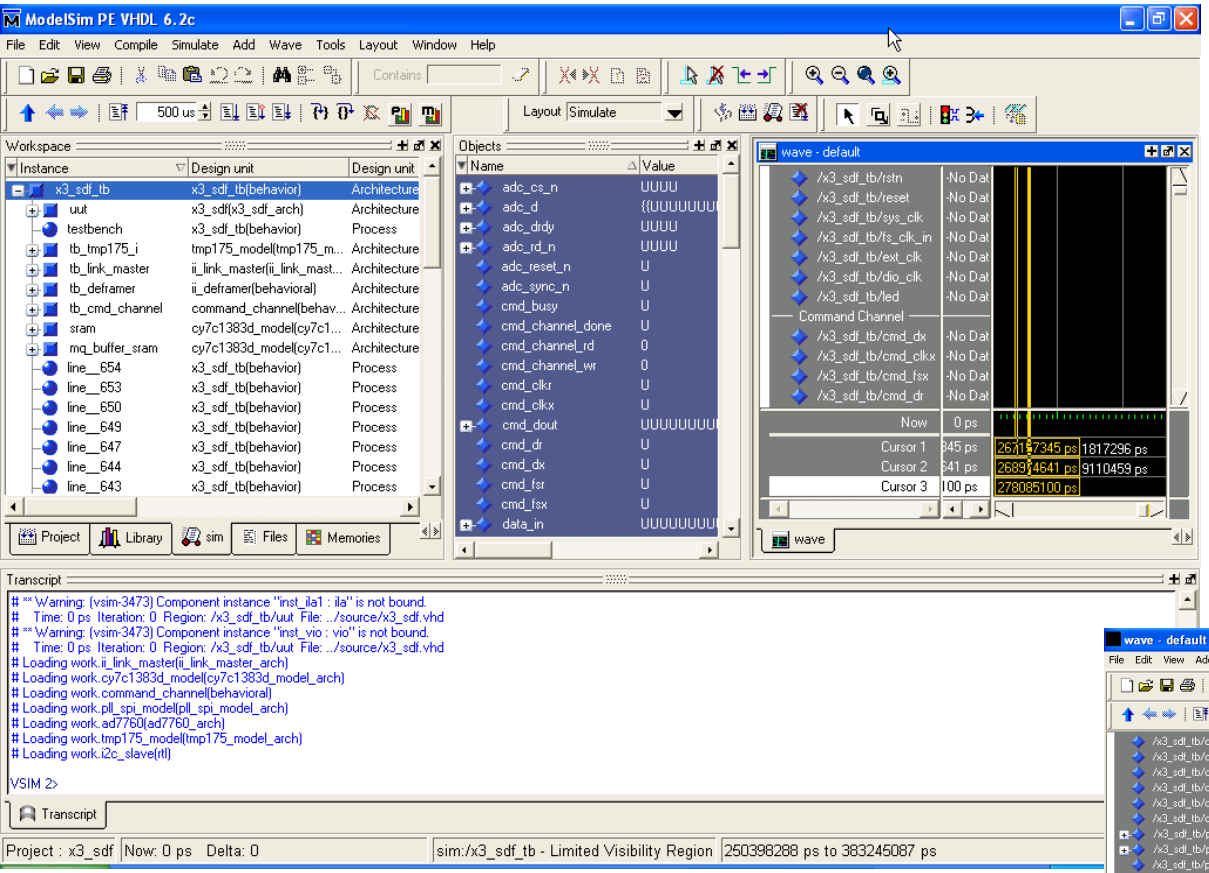
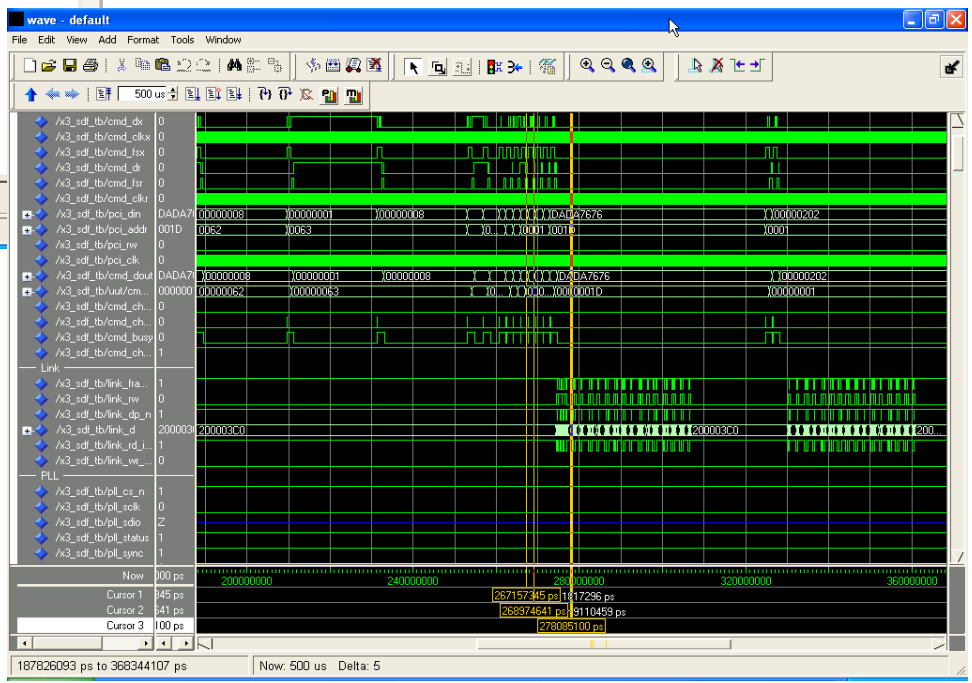
... real time solutions!

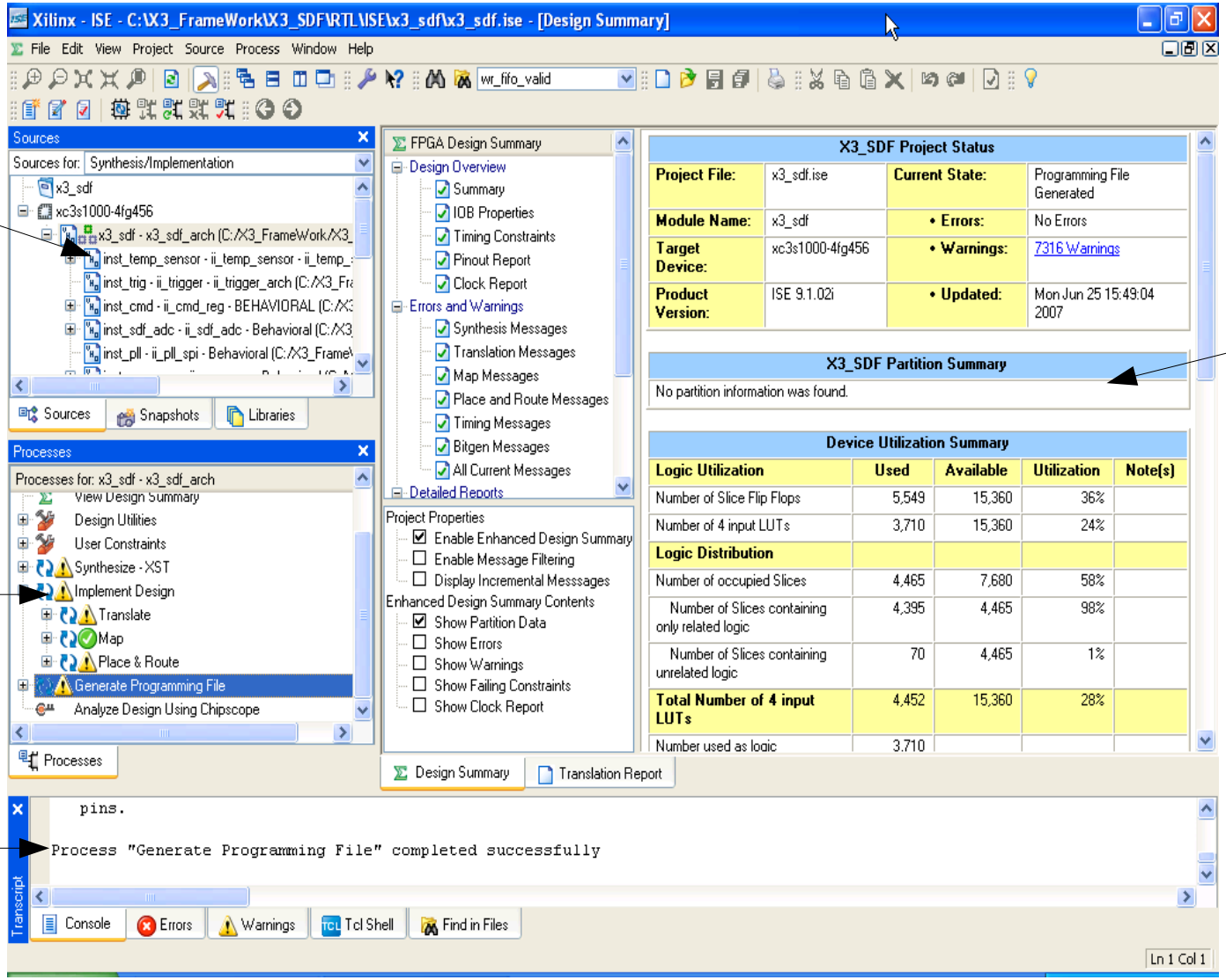


- Simulate the logic using testbench
- FrameWork Logic provides complete testbench with models for A/D, memories, etc
- Saves time before debug!



Xilinx ISE Environment

Innovative Integration
... real time solutions!



Sources

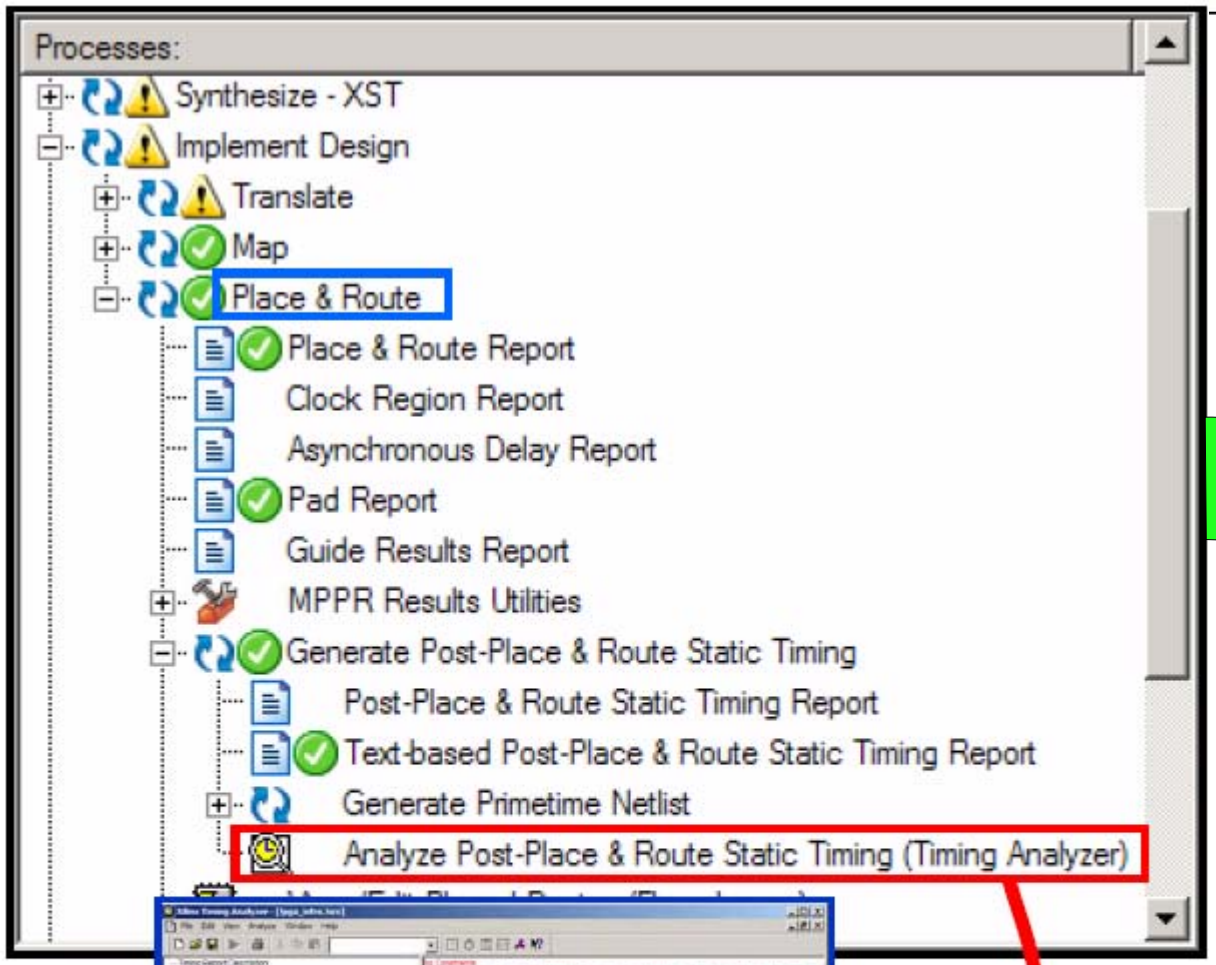
Processes

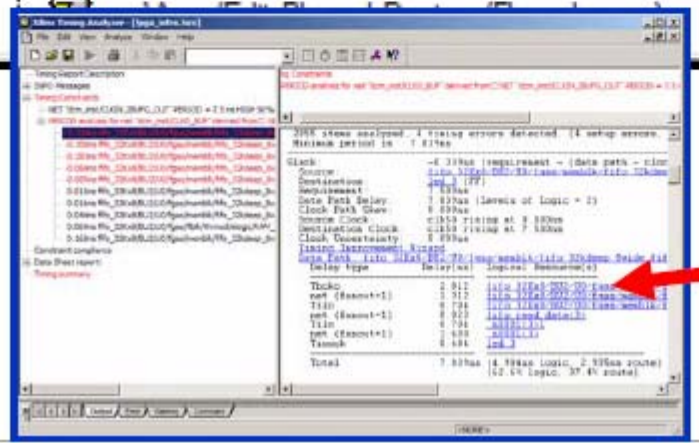
Console

Project Summary

Step 5: Compile and Download Logic

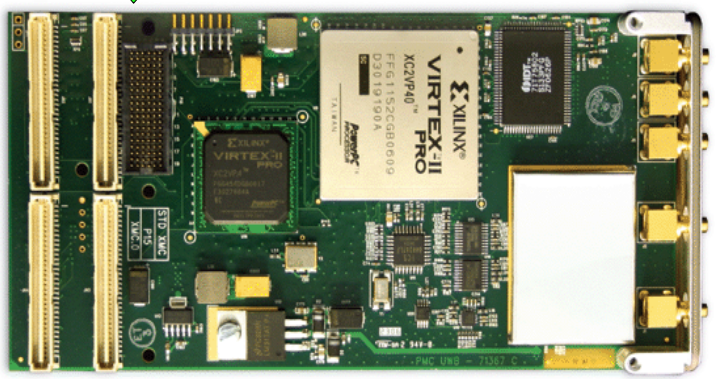
Innovative Integration
... real time solutions!





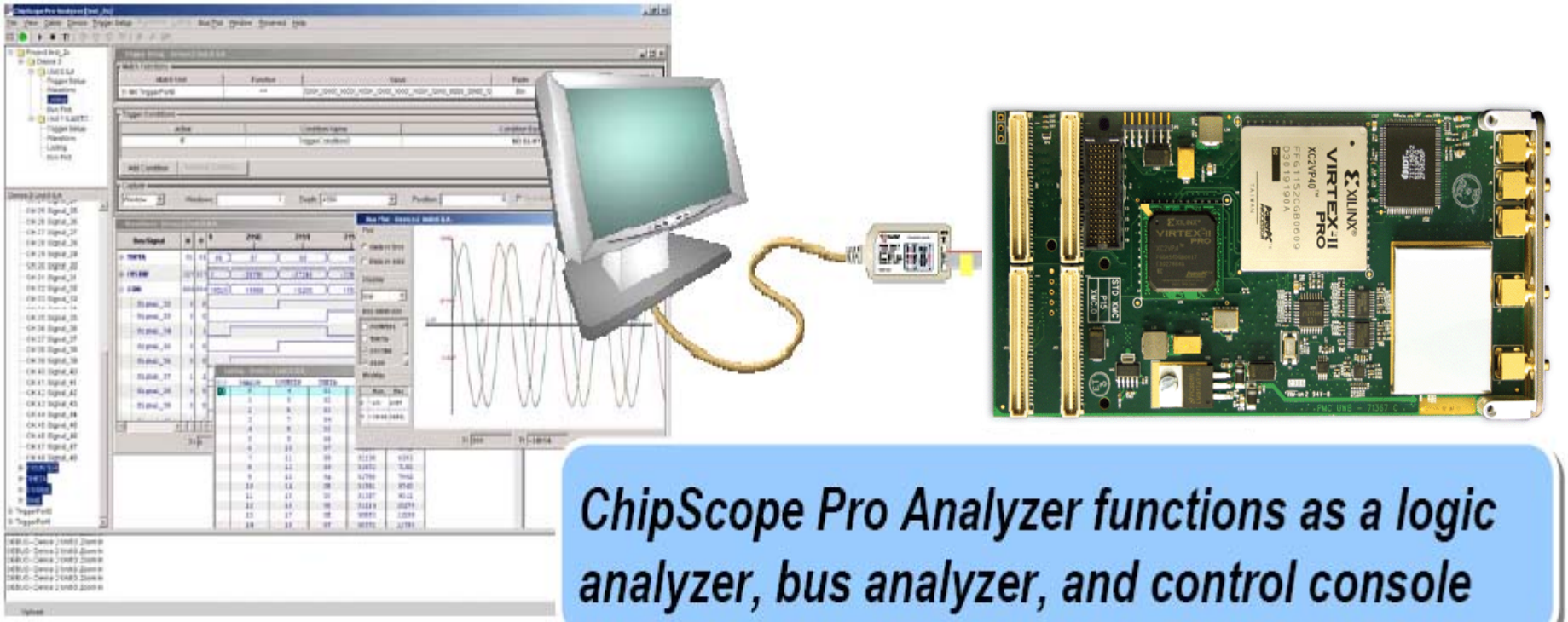
Parallel Cable IV

Platform USB Cable



Step 6 - Debug

Innovative Integration
... real time solutions!



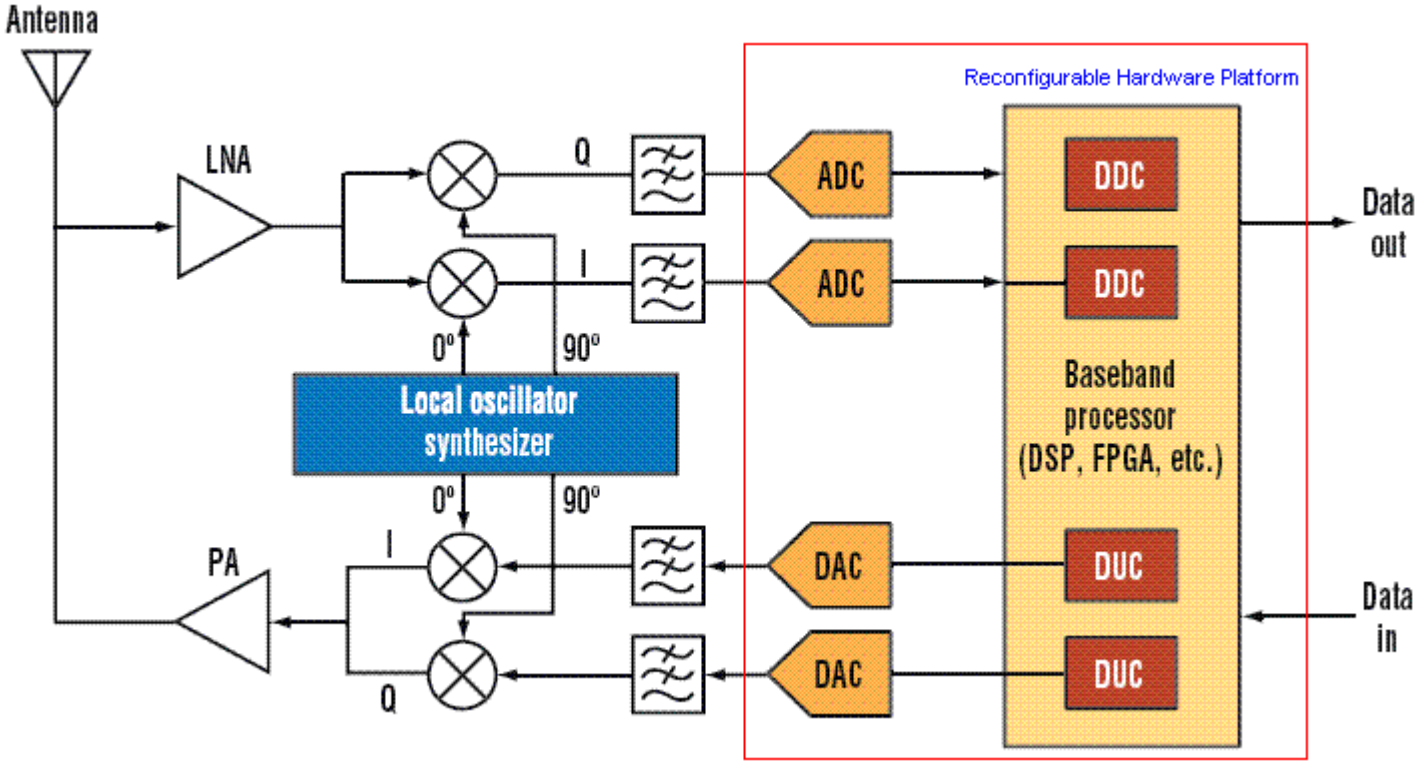
ChipScope Pro Analyzer functions as a logic analyzer, bus analyzer, and control console

Software Defined Radio

Software Defined Radio

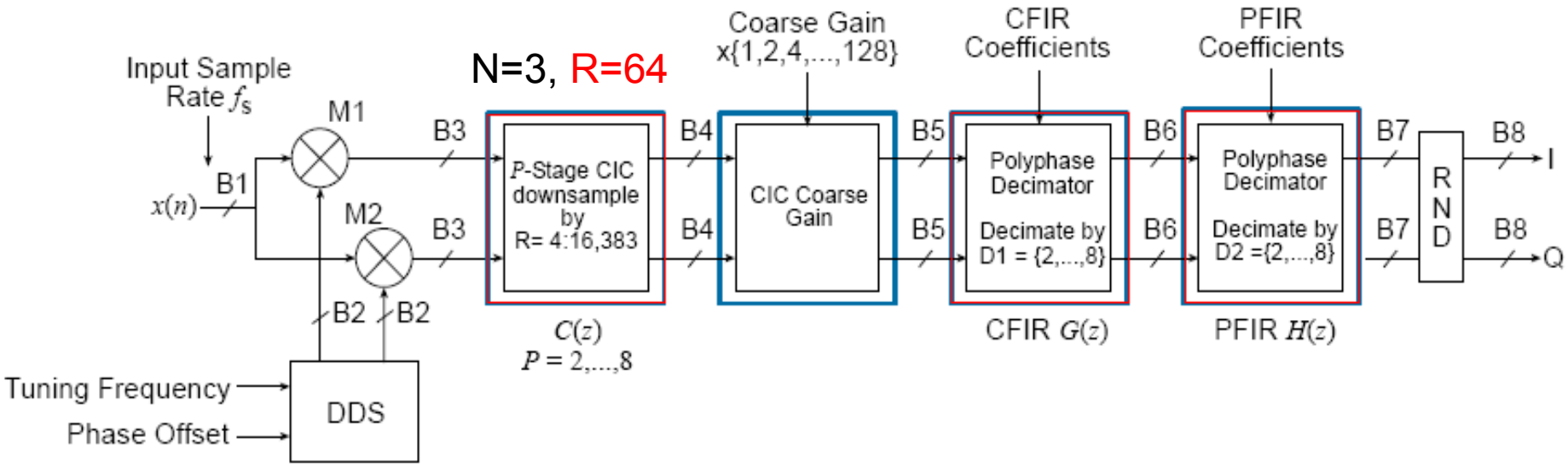
Innovative Integration
... real time solutions!

- Wireless communication issue today
  - Compatibility & Spectrum usage
- Purpose
  - Produce a radio that can receive and transmit a new form of radio protocol by running new software
- Key
  - Software- programmable hardware



Digital Down Converter (DDC)

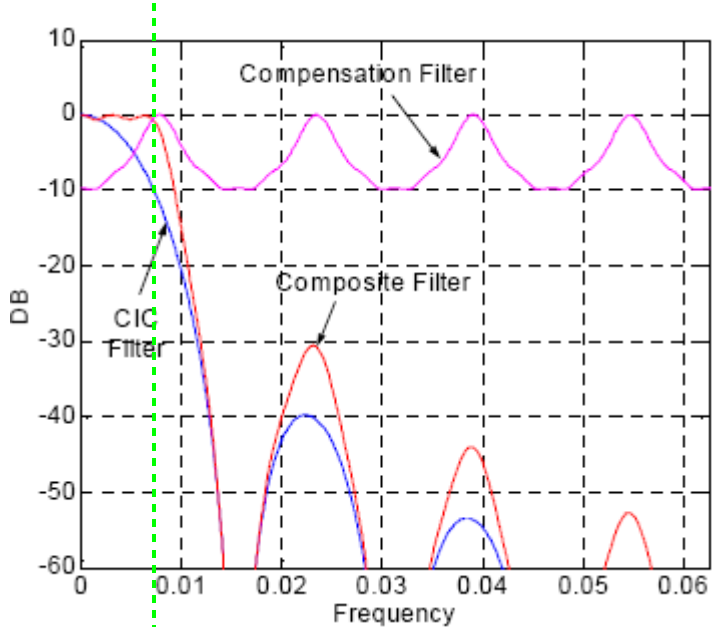
Innovative Integration
... real time solutions!



C(z)

G(z)

B6



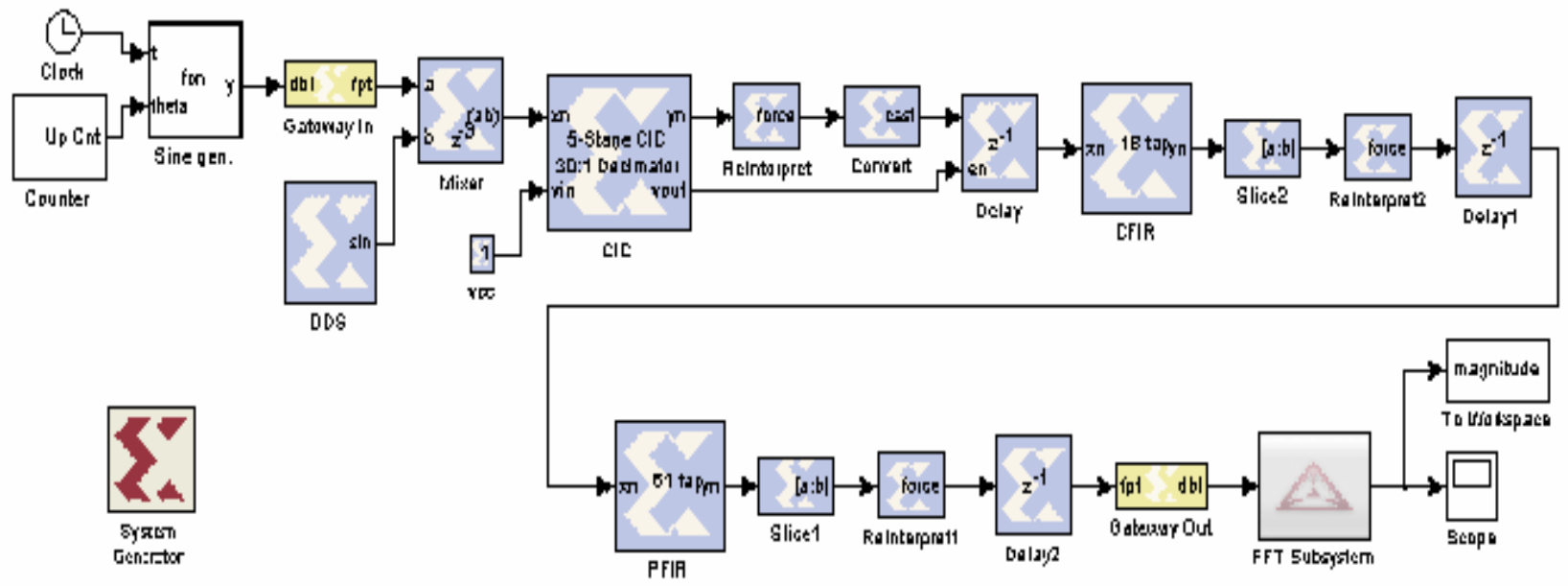
Normalized freq

0.5 / 64 = 0.0078

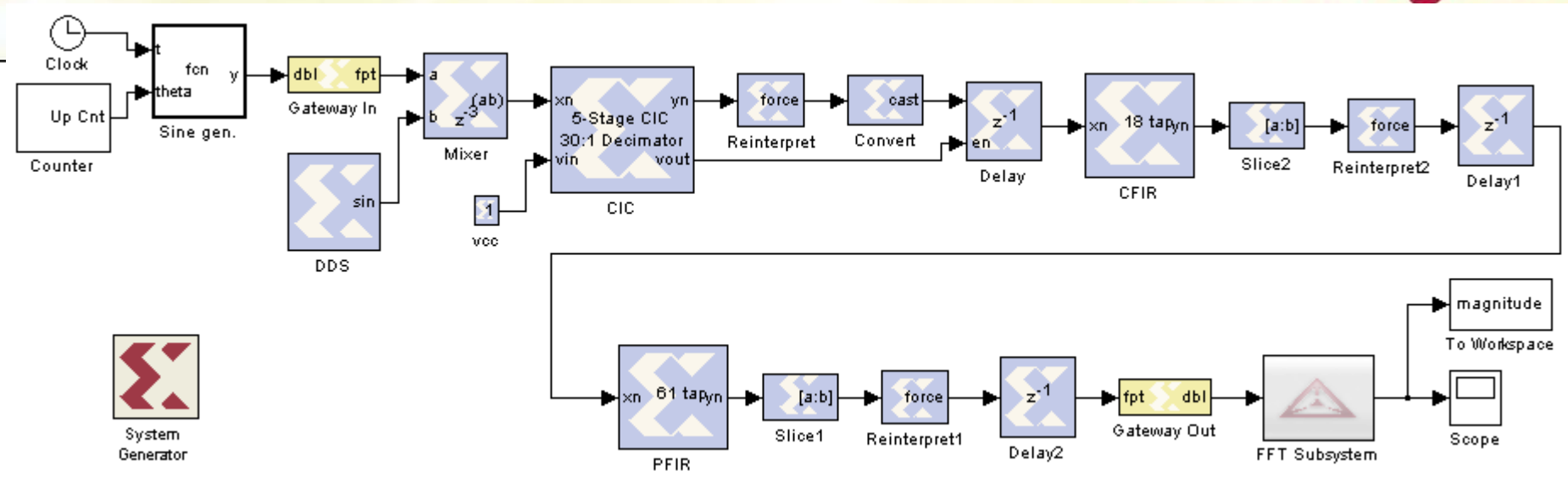
Our DDC Solution

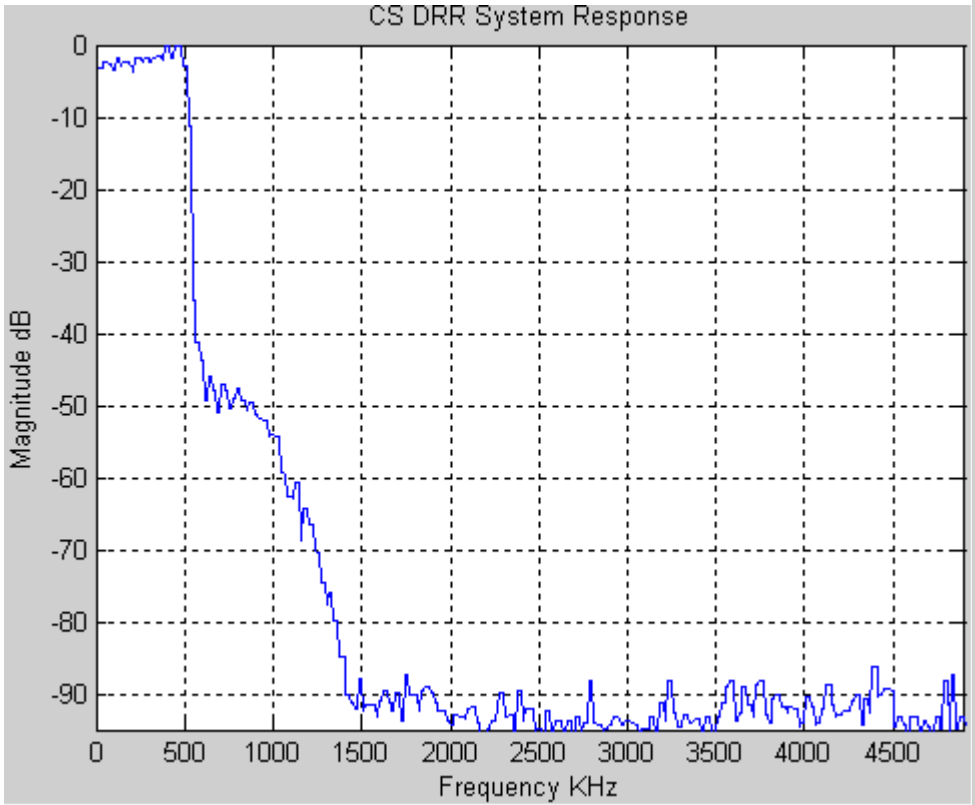
Innovative Integration
... real time solutions!

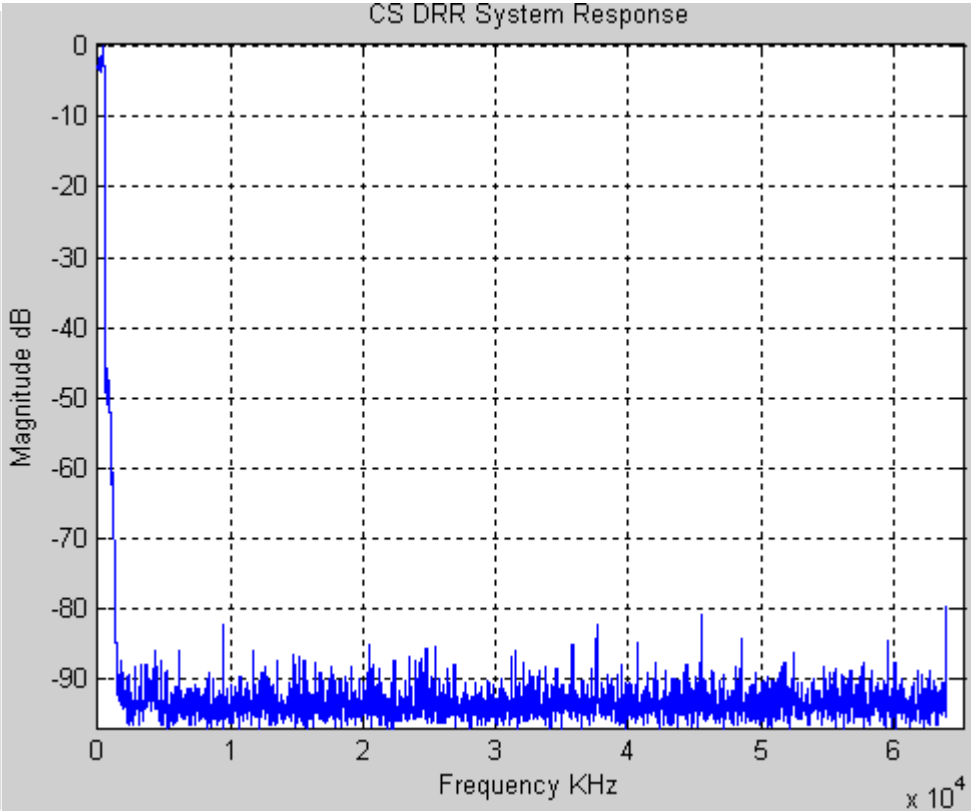
- MATLAB Simulink design for FPGA
- Supports up to 208 MSPS with >90 dB dynamic range
- 10 kHz tuning resolution



MATLAB Simulation (Bit True, Cycle True)

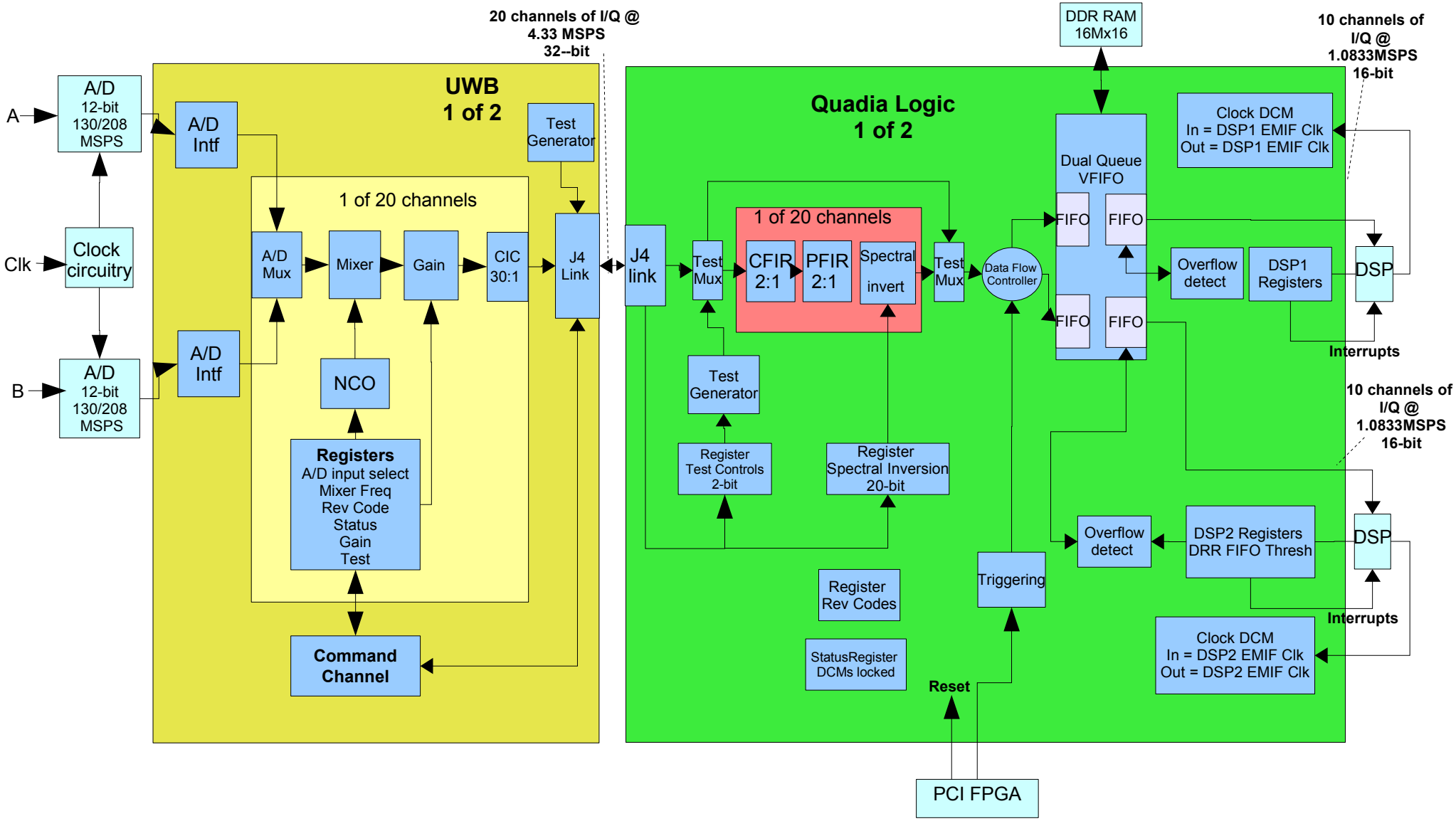






II Digital Receiver (SDR)

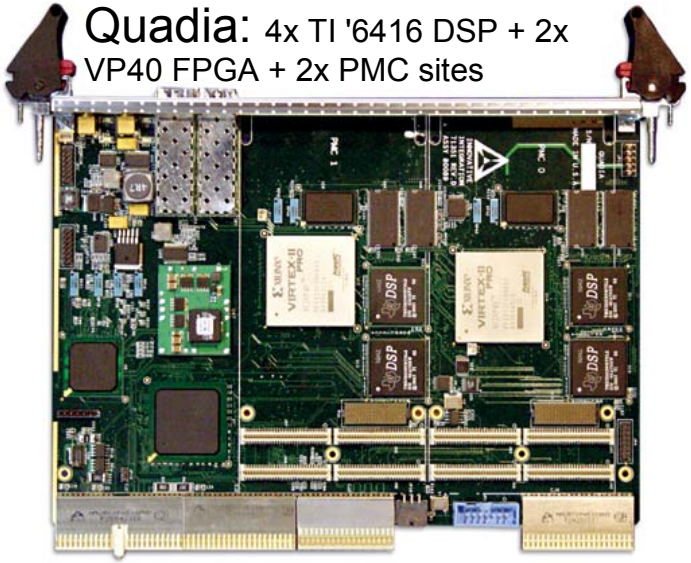
Innovative Integration
... real time solutions!



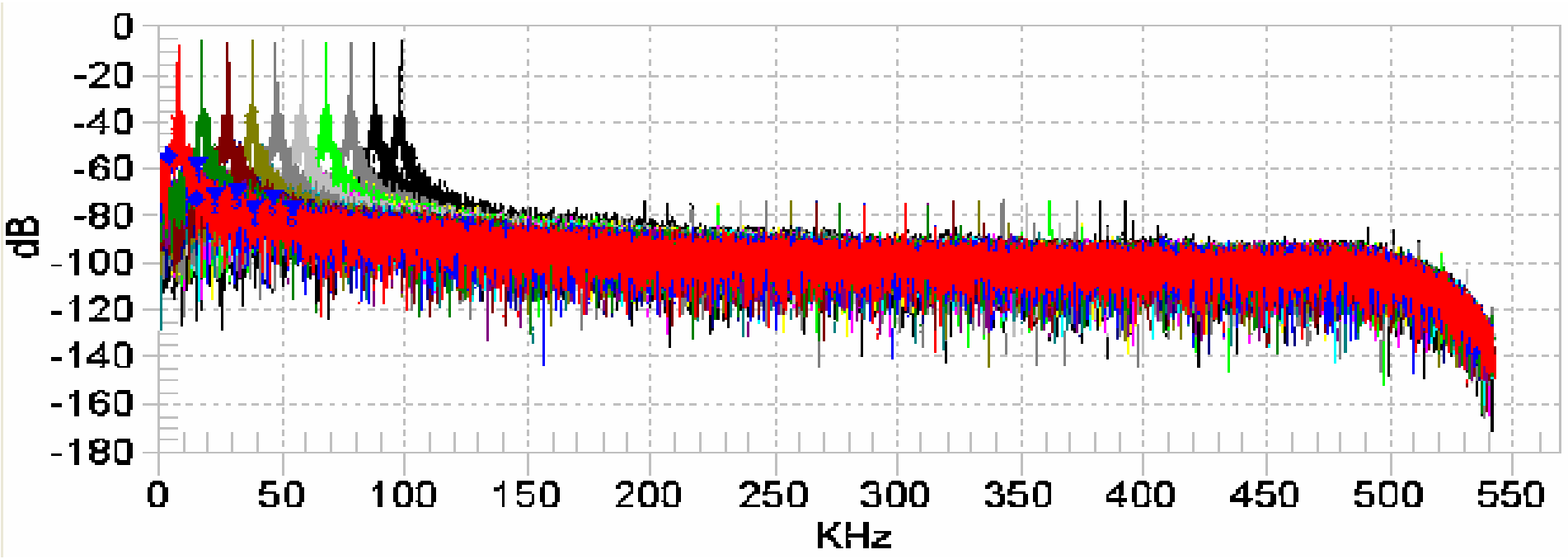
Software Defined Radio Results

Innovative Integration
... real time solutions!

- SDR implemented on Quadia and UWB
- Example results shown for 97.5MHz input, 130 MSPS sampling, channels tuned to 97.5+n*10KHz



PMC UWB:
2x 250 MSPS A/D
+ VP40 FPGA



II SDR Support

- Logic designs and supporting software are available for application development
- Full application note available