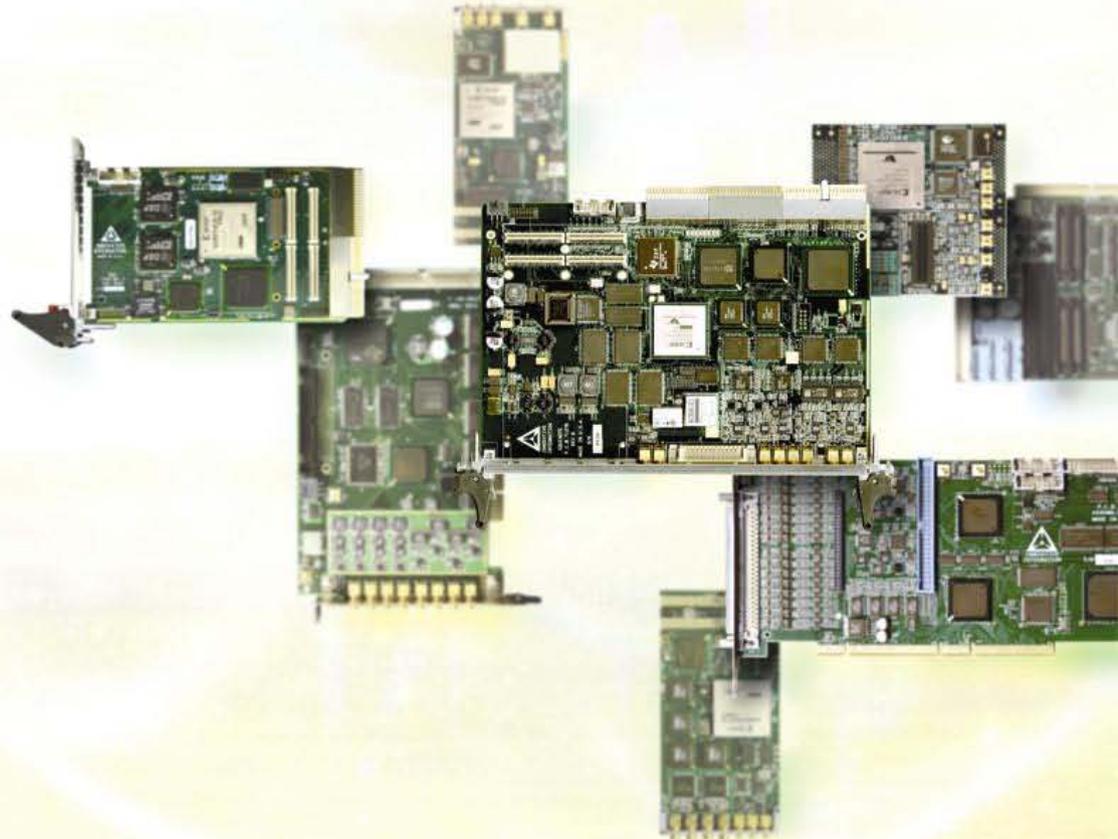


FrameWork Logic and MATLAB Board Support Package

Dan McLane
Billy Kao

Innovative Integration



FrameWork Logic and MATLAB Products



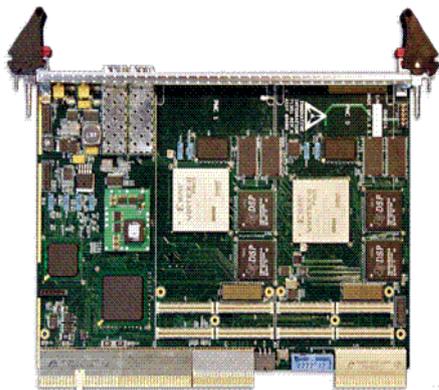
- Innovative Integration offers
 - FrameWork Logic for traditional VHDL design using Xilinx ISE software
 - Support for MATLAB/Simulink and Xilinx System Generator based designs
 - Extensive II VHDL IP cores
- Results
 - Rapid application development
 - Smooth integration of custom logic in II Framework
 - Real time testing and debugging of algorithms using ChipScope Pro and MATLAB/Simulink

MATLAB Board Support Package

Bridge to the Real World - System Generator/Simulink

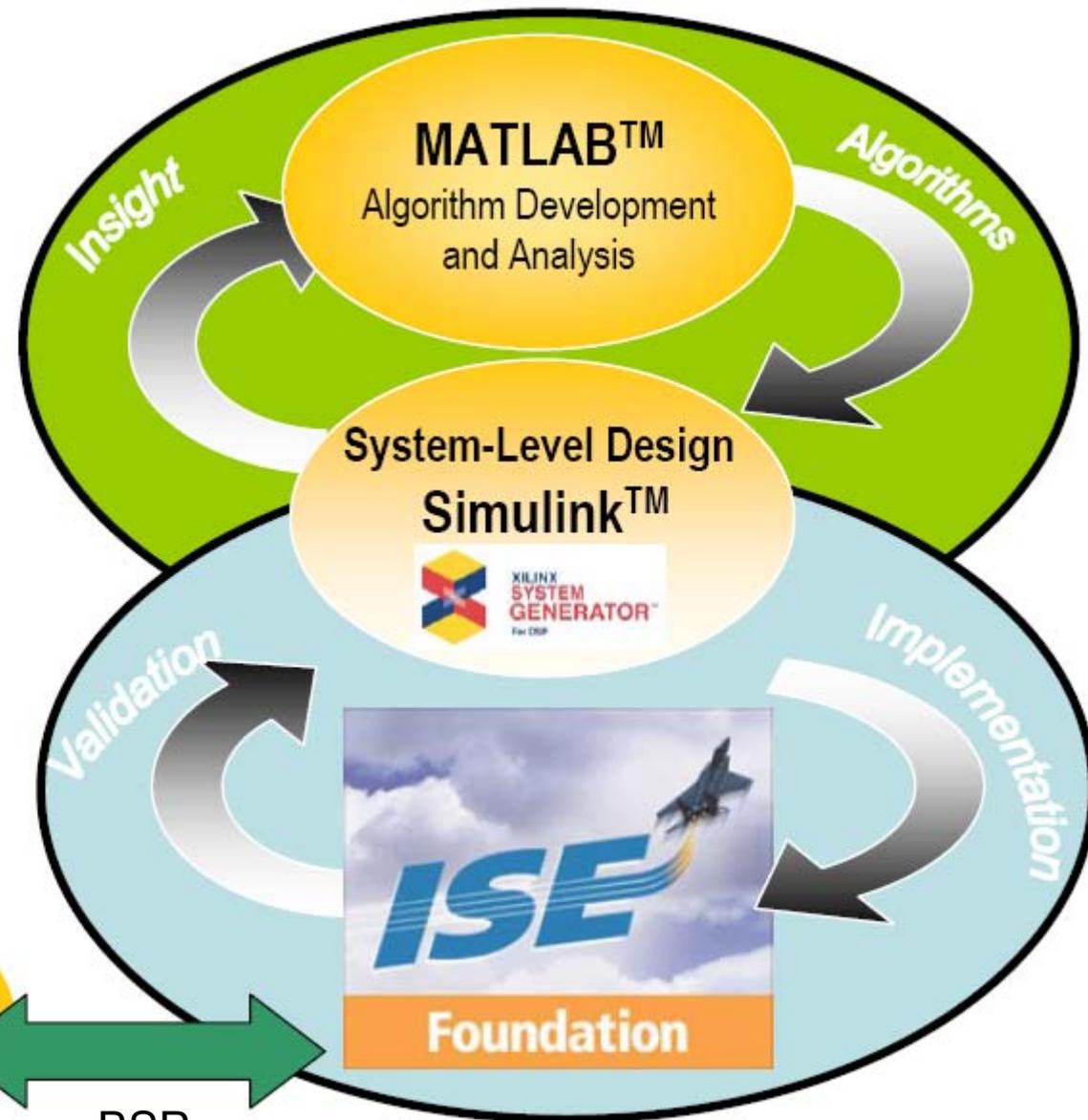
Features

- Bit true, cycle true
- Simulation => Validation
=> Implementation in
Simulink environment
- Hardware-in-the-loop

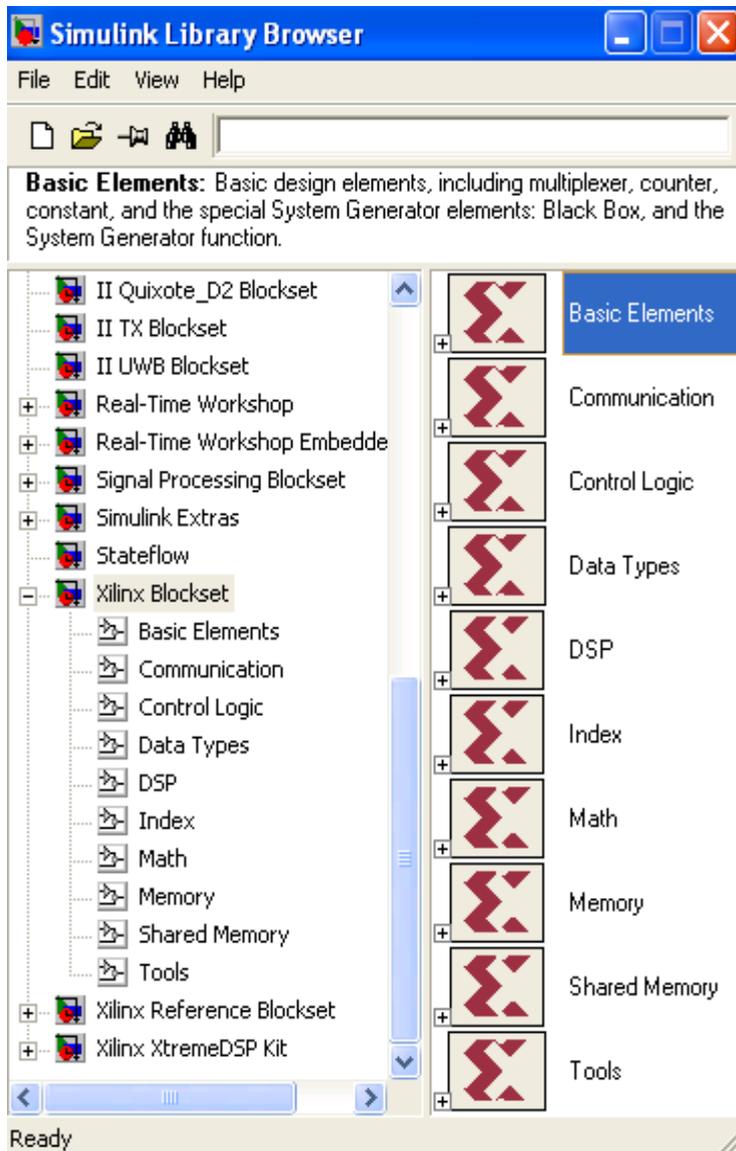


3rd party prototype
and development
boards

BSP



Start Your Design in Simulink



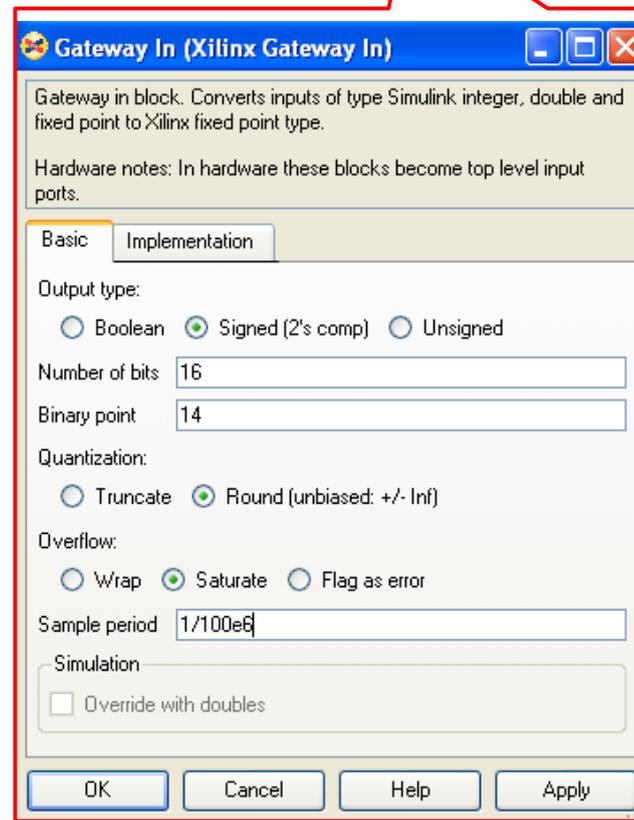
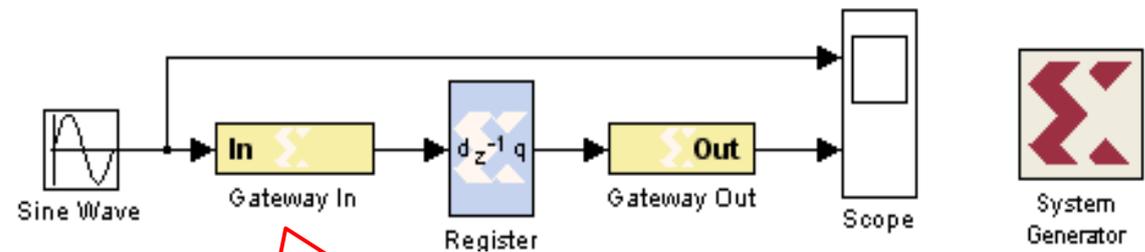
Simulink Library Browser

File Edit View Help

Basic Elements: Basic design elements, including multiplexer, counter, constant, and the special System Generator elements: Black Box, and the System Generator function.

- II Quixote_D2 Blockset
- II TX Blockset
- II UWB Blockset
- Real-Time Workshop
- Real-Time Workshop Embedde
- Signal Processing Blockset
- Simulink Extras
- Stateflow
- Xilinx Blockset
 - Basic Elements
 - Communication
 - Control Logic
 - Data Types
 - DSP
 - Index
 - Math
 - Memory
 - Shared Memory
 - Tools
- Xilinx Reference Blockset
- Xilinx XtremeDSP Kit

Ready



Gateway In (Xilinx Gateway In)

Gateway in block. Converts inputs of type Simulink integer, double and fixed point to Xilinx fixed point type.

Hardware notes: In hardware these blocks become top level input ports.

Basic Implementation

Output type:
 Boolean Signed (2's comp) Unsigned

Number of bits: 16

Binary point: 14

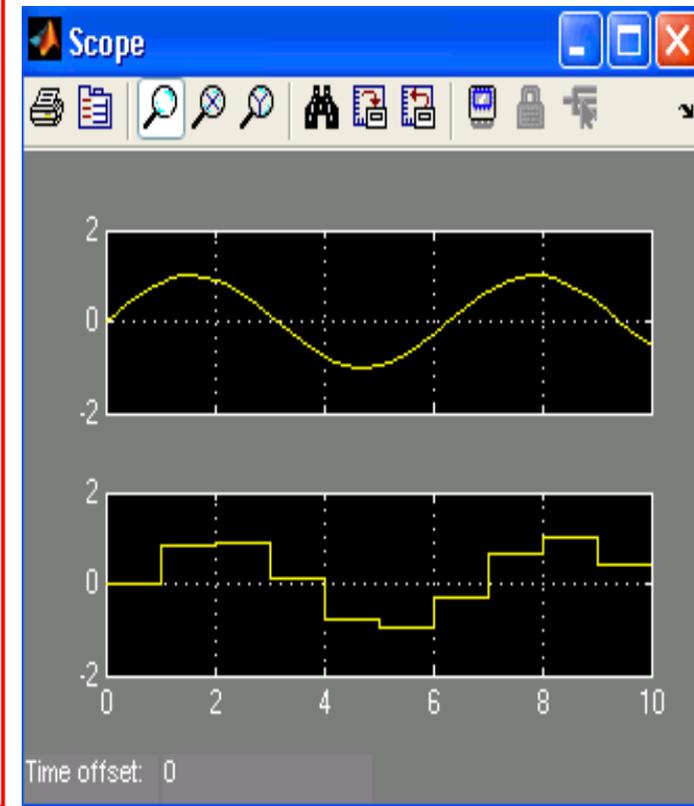
Quantization:
 Truncate Round (unbiased: +/- Inf)

Overflow:
 Wrap Saturate Flag as error

Sample period: 1/100e6

Simulation
 Override with doubles

OK Cancel Help Apply



Xilinx System Generator



Library: xbs_r4

File Edit View Format Help

Xilinx Blockset v8.2
(c) 2006 Xilinx, Inc.

- Basic Elements
- Communication
- Control Logic
- DSP
- Data Types
- Index
- Math
- Memory
- Shared Memory
- Tools

Ready 100% Locked

Library: xbsBasic_r4 *

File Edit View Format Help

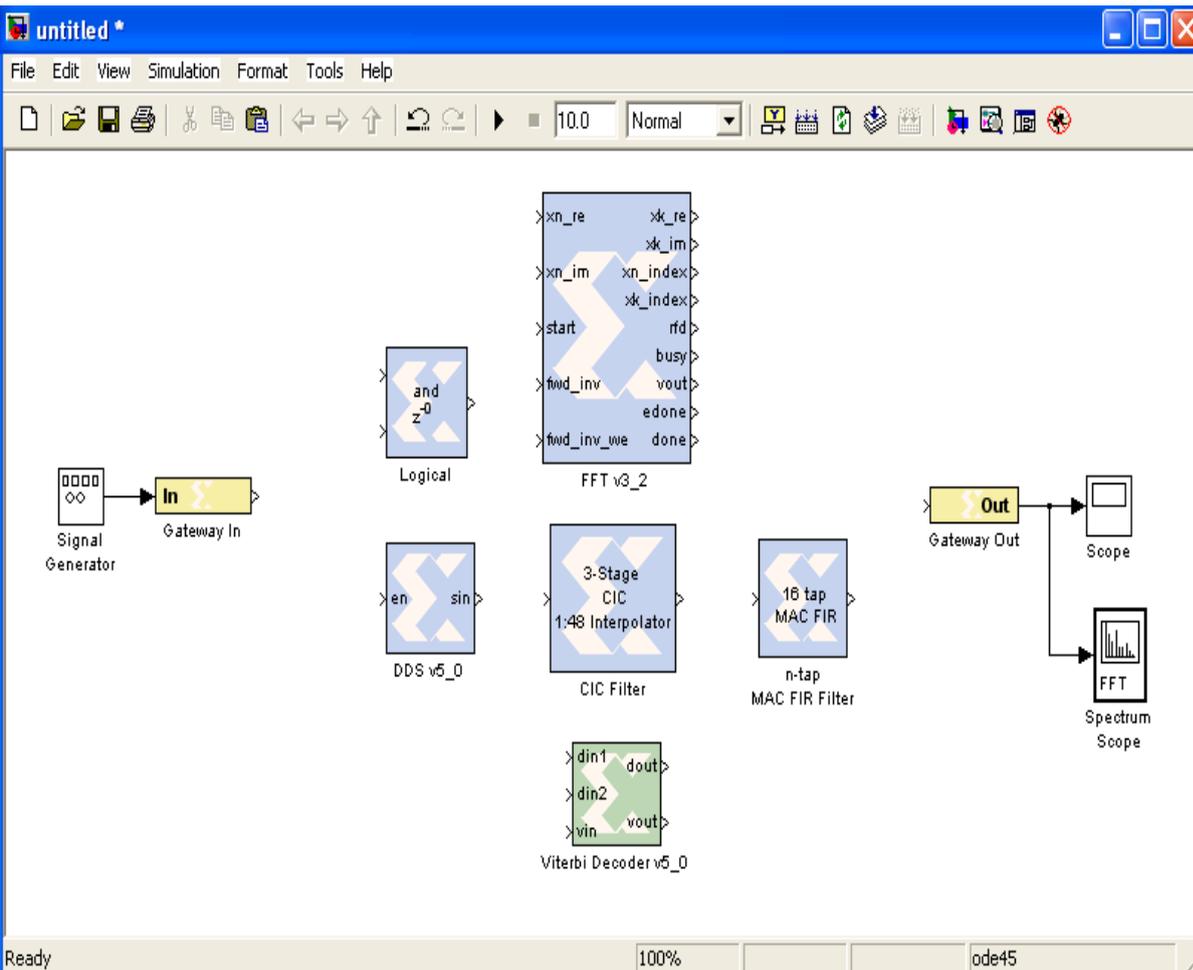
Xilinx Blockset v8.2
(c) 2006 Xilinx, Inc.

Basic Library

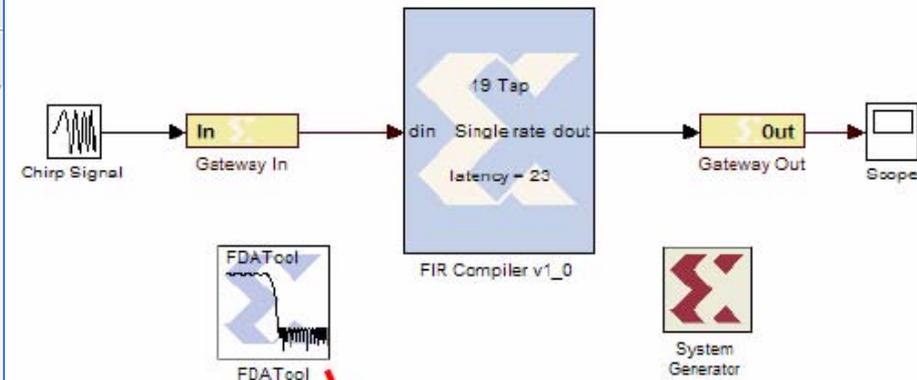
- System Addressable Shift Register
- Assert
- BitBasher
- Black Box
- Time Division Demultiplexer
- Time Division Multiplexer
- Up Sample
- Clock Enable Probe
- Concat
- Constant
- Convert
- Counter
- Register
- Reinterpret
- Relational
- Delay
- Down Sample
- Expression
- Gateway In
- Gateway Out
- Serial to Parallel
- Slice
- Inverter
- LFSR
- Logical
- Mux
- Parallel to Serial

Ready 100% Unlocked

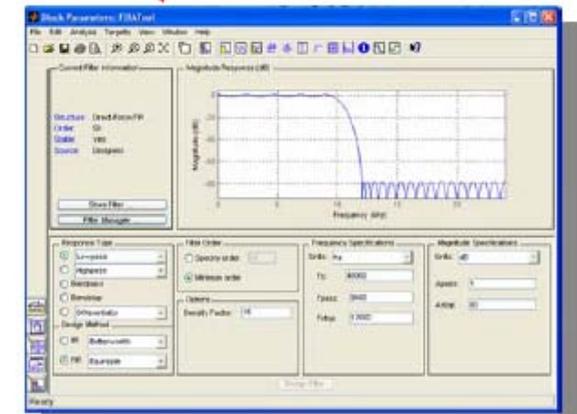
System Modeling in Simulink



FIR Compiler

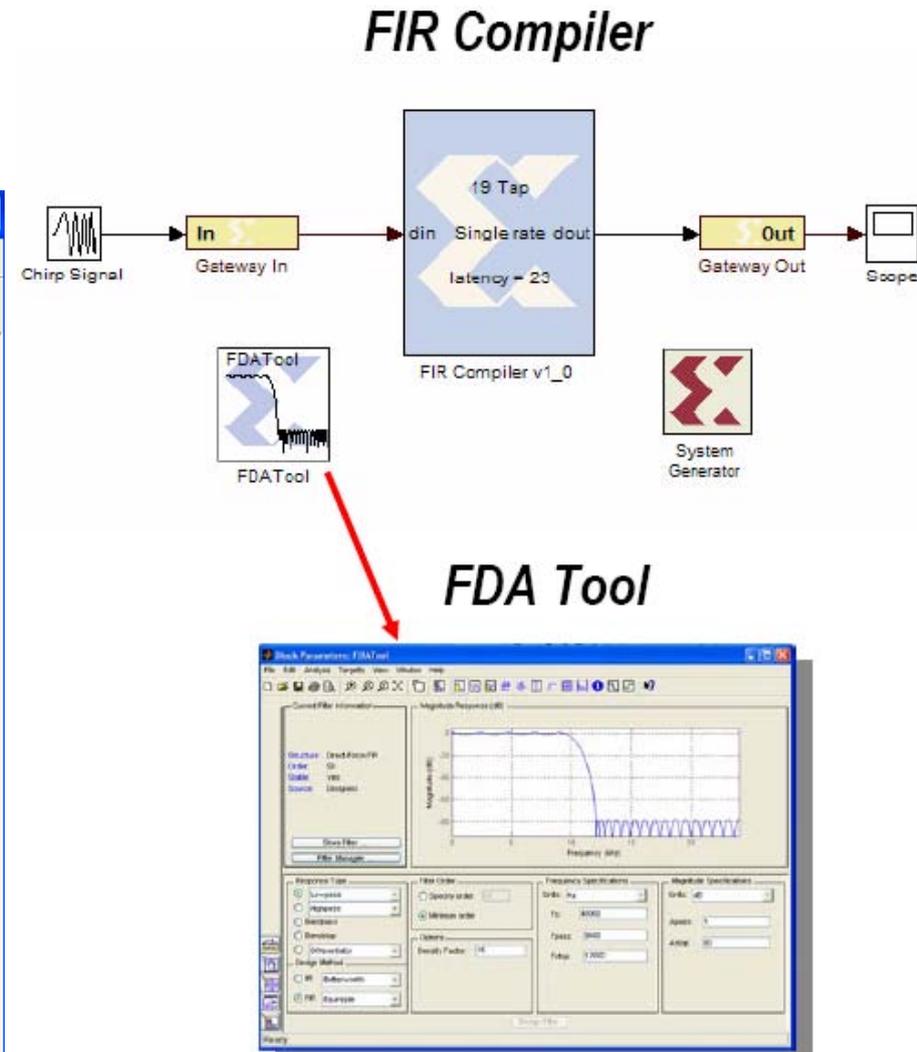
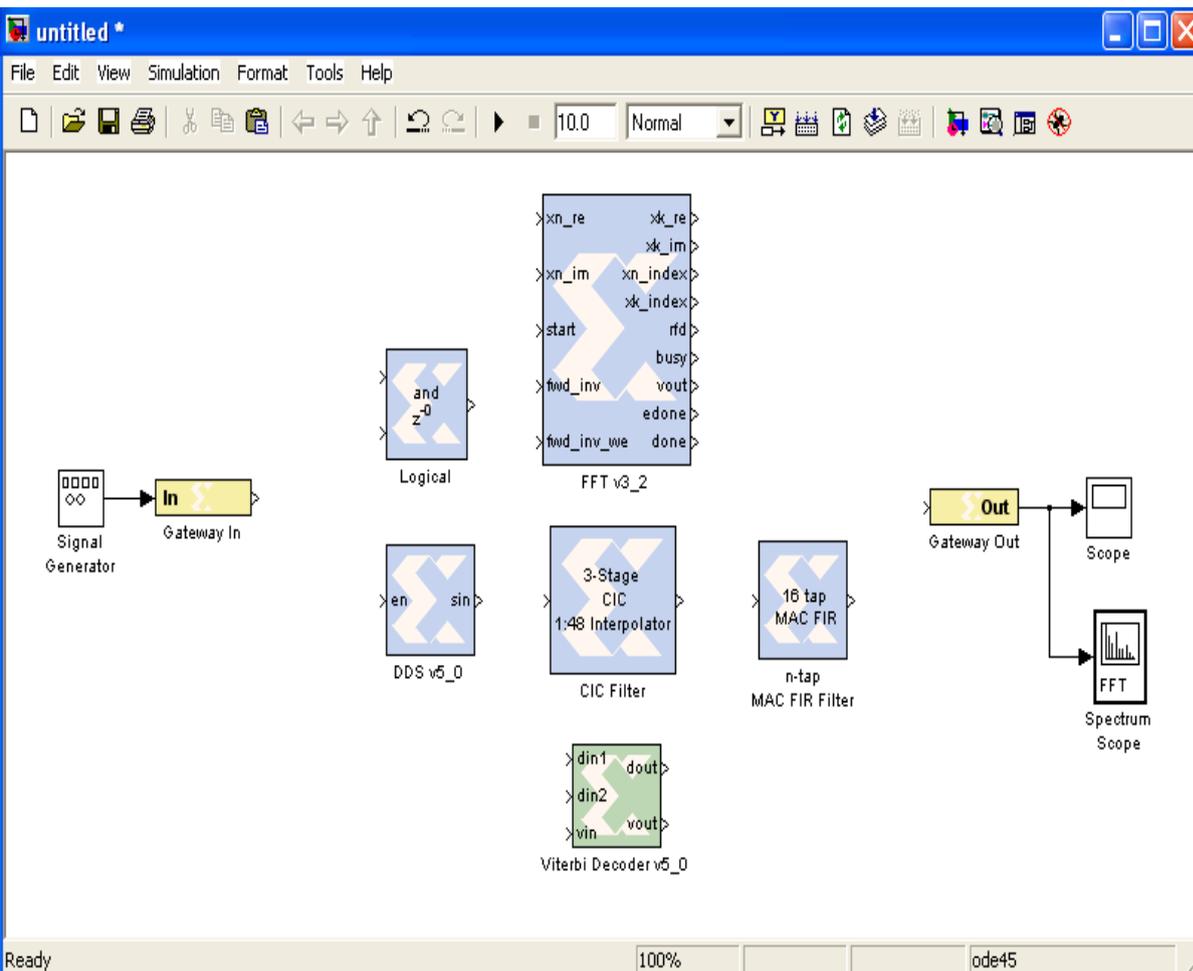


FDA Tool

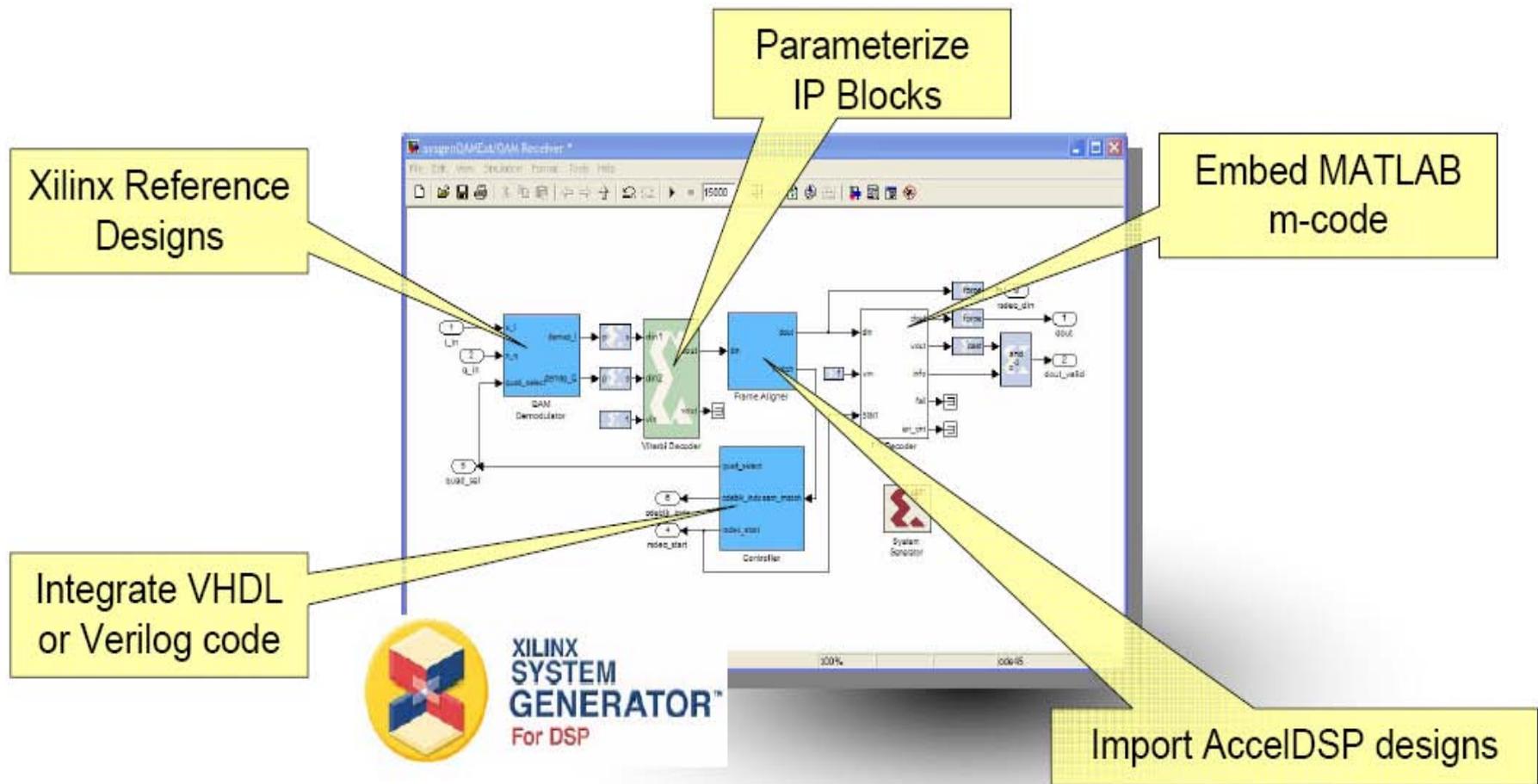


System Modeling in Simulink

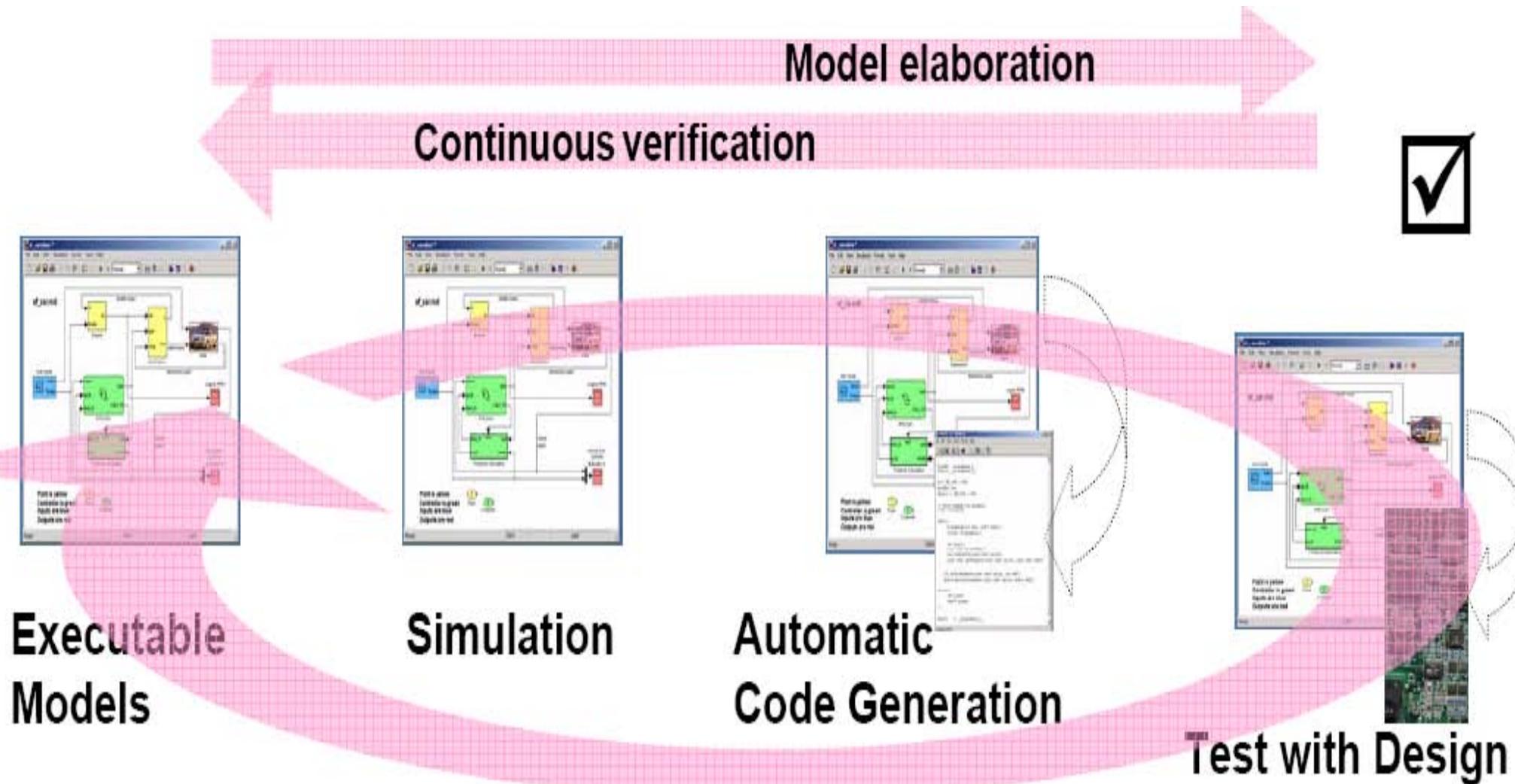
- Visualized debugging tools
- Reliable IP cores
- No multiple clock domain issues



Cores from Various Sources



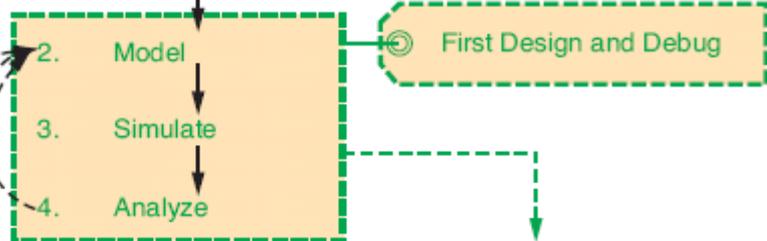
Design Flow in Simulink



Design Flow Comparison

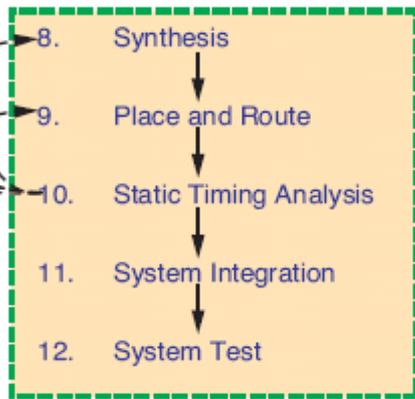
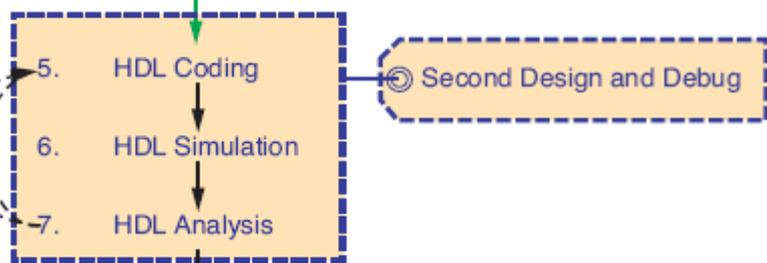
System Engineering

1. Specification



• Hardware Spec
• Test Vectors

Hardware Engineering



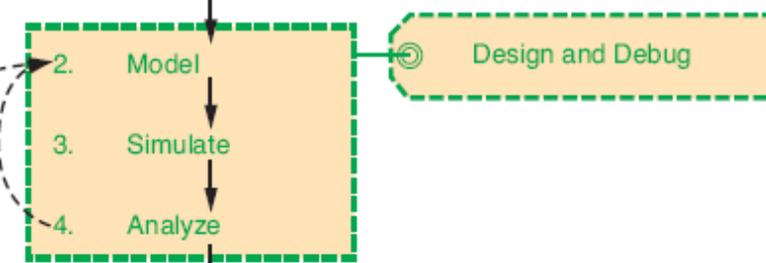
Physical Design

Traditional VHDL Coding

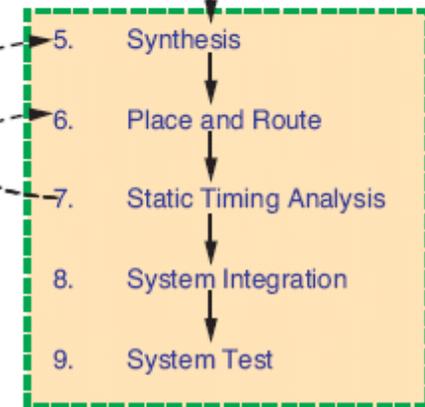
- System level design, no hardware engineer needed

System & Algorithm Design

1. Specification



Physical Design



Xilinx System Generator

II MATLAB BSP

Advantage

- Save more than 80% time of hand-coding VHDL

System Generator : 45.5 hrs

Traditional VHDL : 782 hrs

Reason: clocking, defect discovery, and component interfaces

- Graphical interfaces for easy project construction
- Visual tools for easy debugging
- Fast simulation ability (Support Modelsim and Chipscope)
- Free

Now support: Quadia, Quixote, PMC UWB, TX, DR, P25M, X3
Family

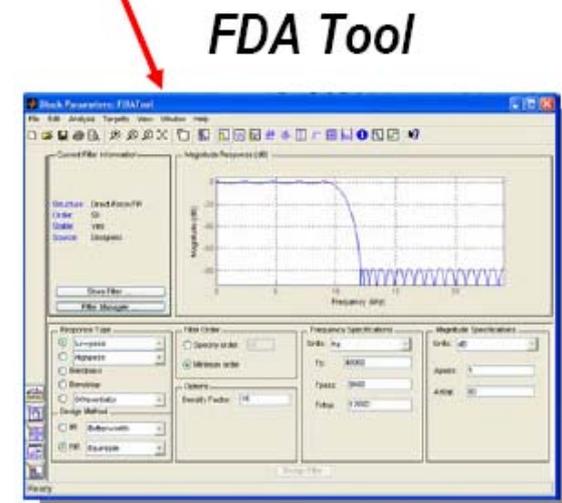
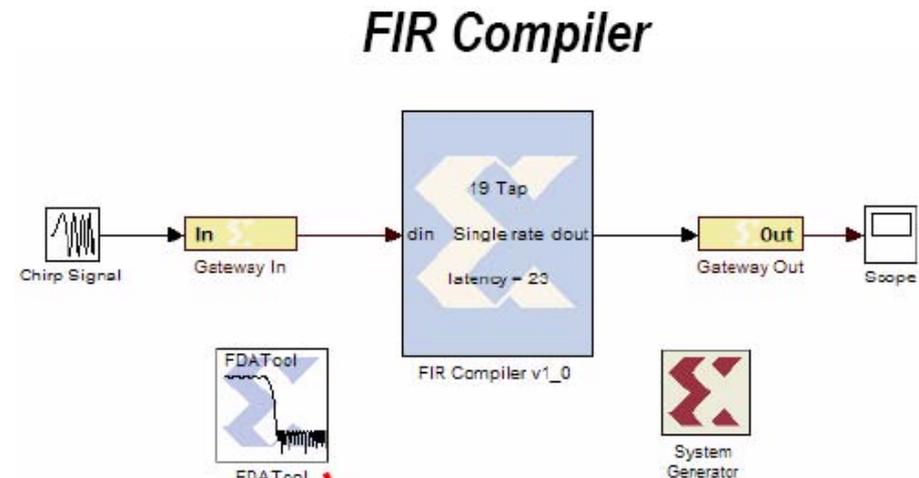
MATLAB BSP Reduces Verification Time



Design	Simulation Time (Seconds)		
	Software	HW Co-Sim	Increase
Beamformer	113	2.5	45X
OFDM BER Test	742	.75	989X
DUC CFR	731	23	32X
Color Space Converter	277	4	69x
Video Scalar	10422	92	113X

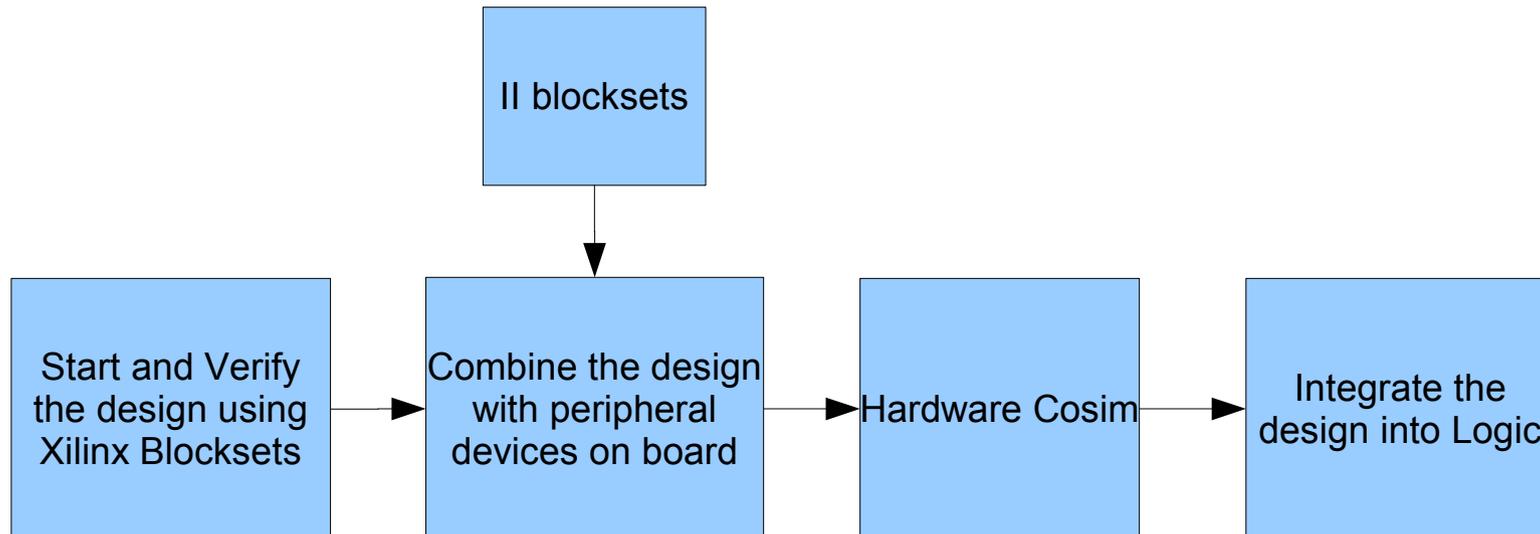
Co-Sim Integrates MATLAB Design Tools with Hardware

- Access the hardware *DIRECTLY* from MATLAB
- Use powerful MATLAB tools for DSP design and test
- Xilinx System Generator tools link Simulink to the hardware through the BSP
- Hardware Co-simulation radically improves system design and test by reducing design and debug effort

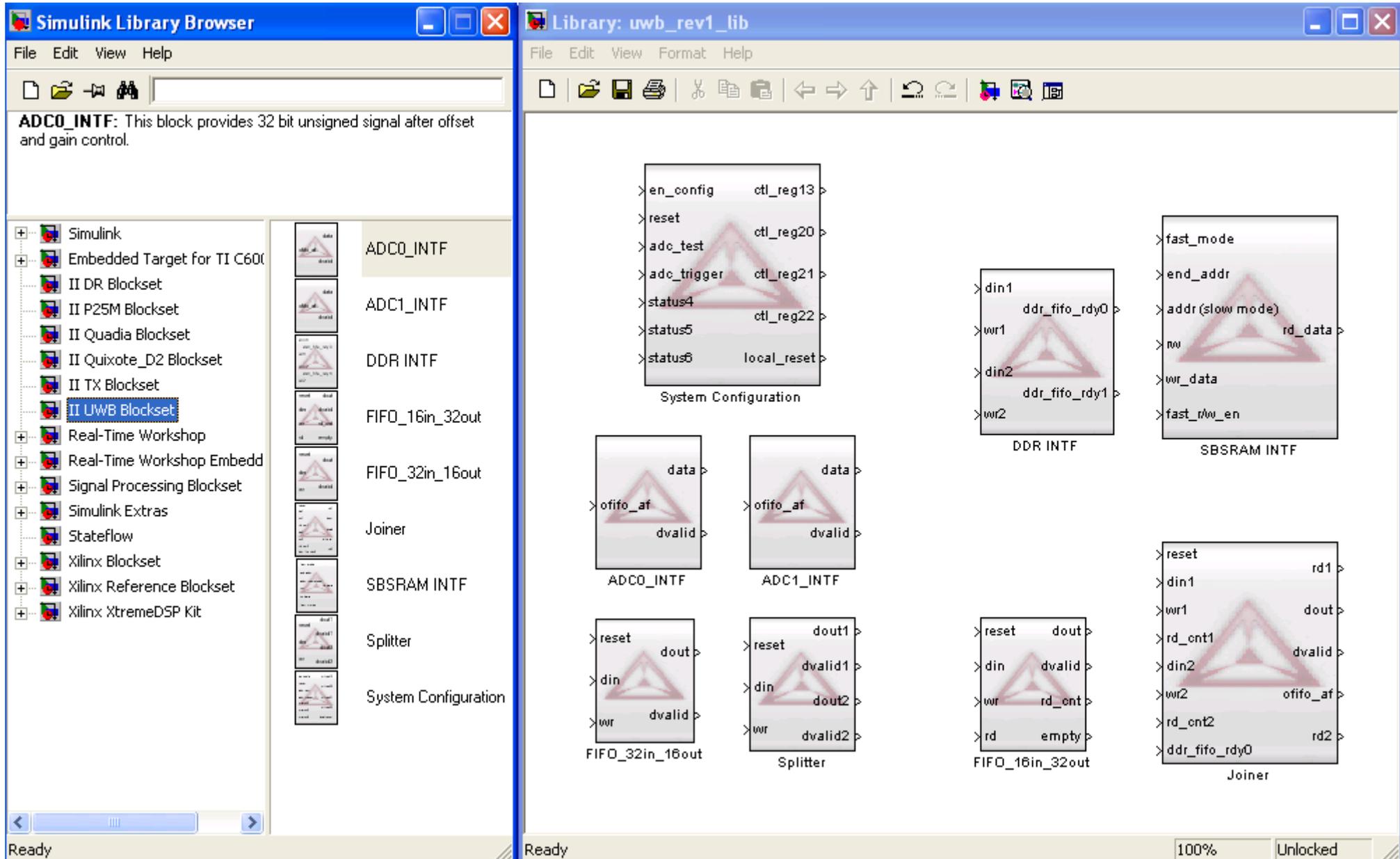


Design Flow

- Step 1. Start your design in Simulink
- Step 2. Attach II blocks to the design
- Step 3. Hardware co-simulation
- Step 4. Implementation



II PMC UWB Library



The image displays two Simulink Library Browser windows. The left window, titled "Simulink Library Browser", shows a tree view of the library structure. The "II UWB Blockset" is selected, and its contents are listed on the right. The right window, titled "Library: uwb_rev1_lib", shows a grid of block icons with their respective input and output ports.

Simulink Library Browser (Left Window):

- File Edit View Help
- ADC0_INTF: This block provides 32 bit unsigned signal after offset and gain control.
- Simulink
- Embedded Target for TI C600
- II DR Blockset
- II P25M Blockset
- II Quadia Blockset
- II Quixote_D2 Blockset
- II TX Blockset
- II UWB Blockset**
- Real-Time Workshop
- Real-Time Workshop Embedd
- Signal Processing Blockset
- Simulink Extras
- Stateflow
- Xilinx Blockset
- Xilinx Reference Blockset
- Xilinx XtremeDSP Kit

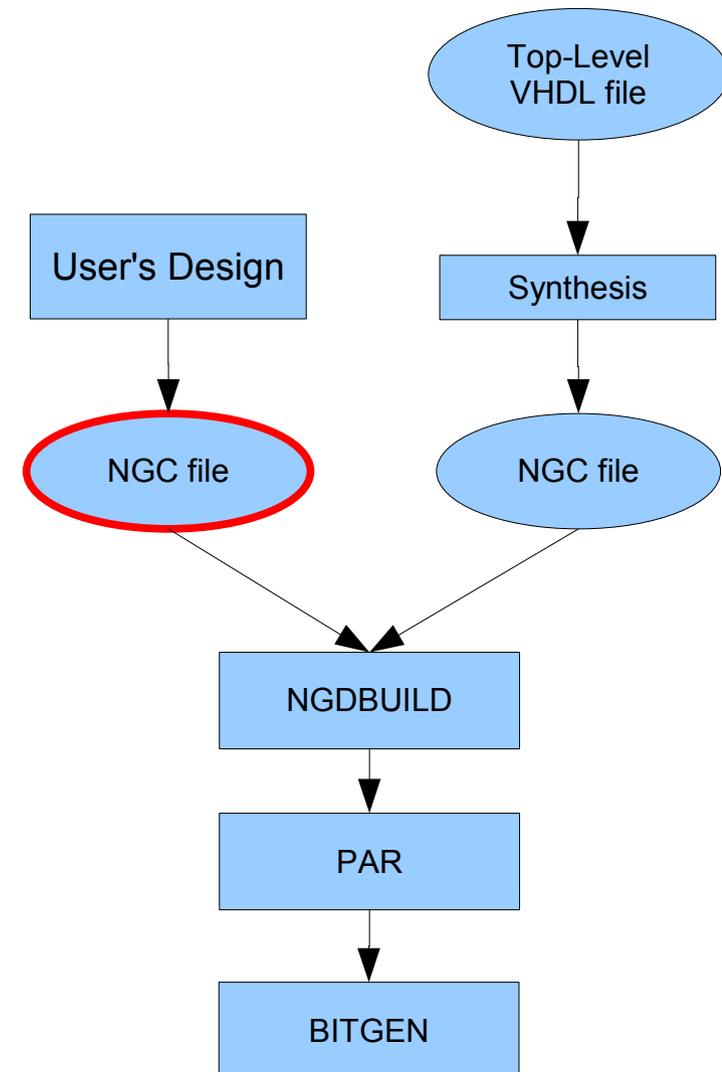
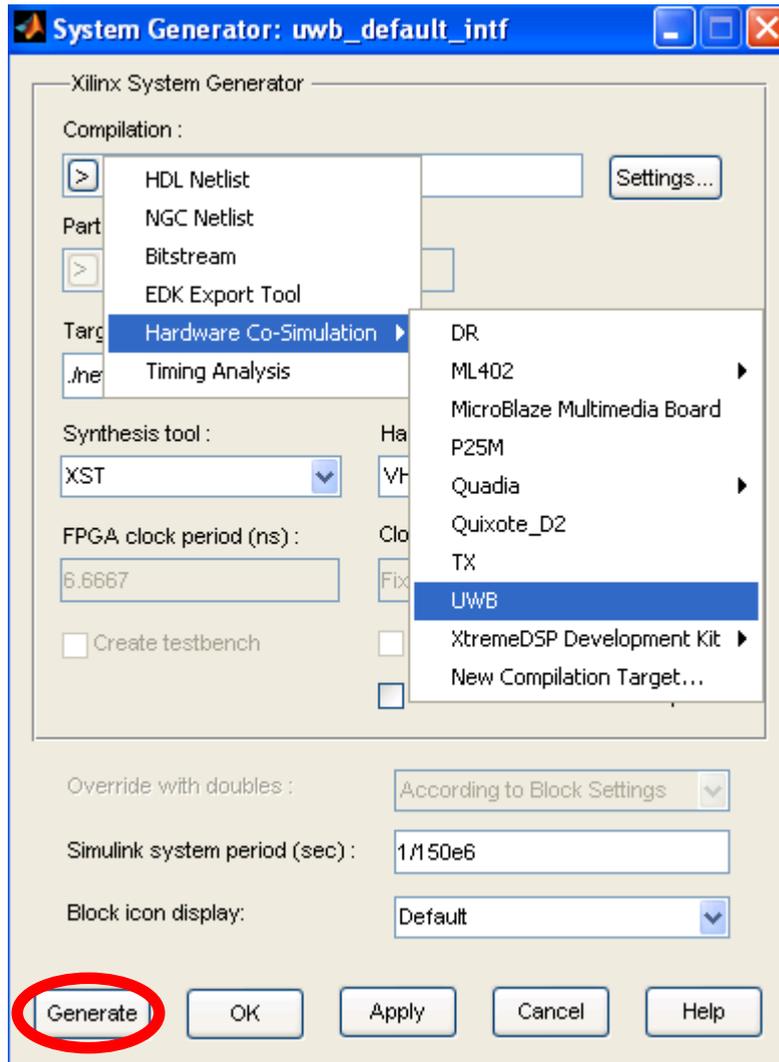
Library: uwb_rev1_lib (Right Window):

- File Edit View Format Help
- System Configuration
- ADC0_INTF
- ADC1_INTF
- DDR INTF
- SBSRAM INTF
- FIFO_16in_32out
- FIFO_32in_16out
- Joiner
- Splitter
- FIFO_32in_16out
- Splitter
- FIFO_16in_32out
- Joiner

Block Port Details:

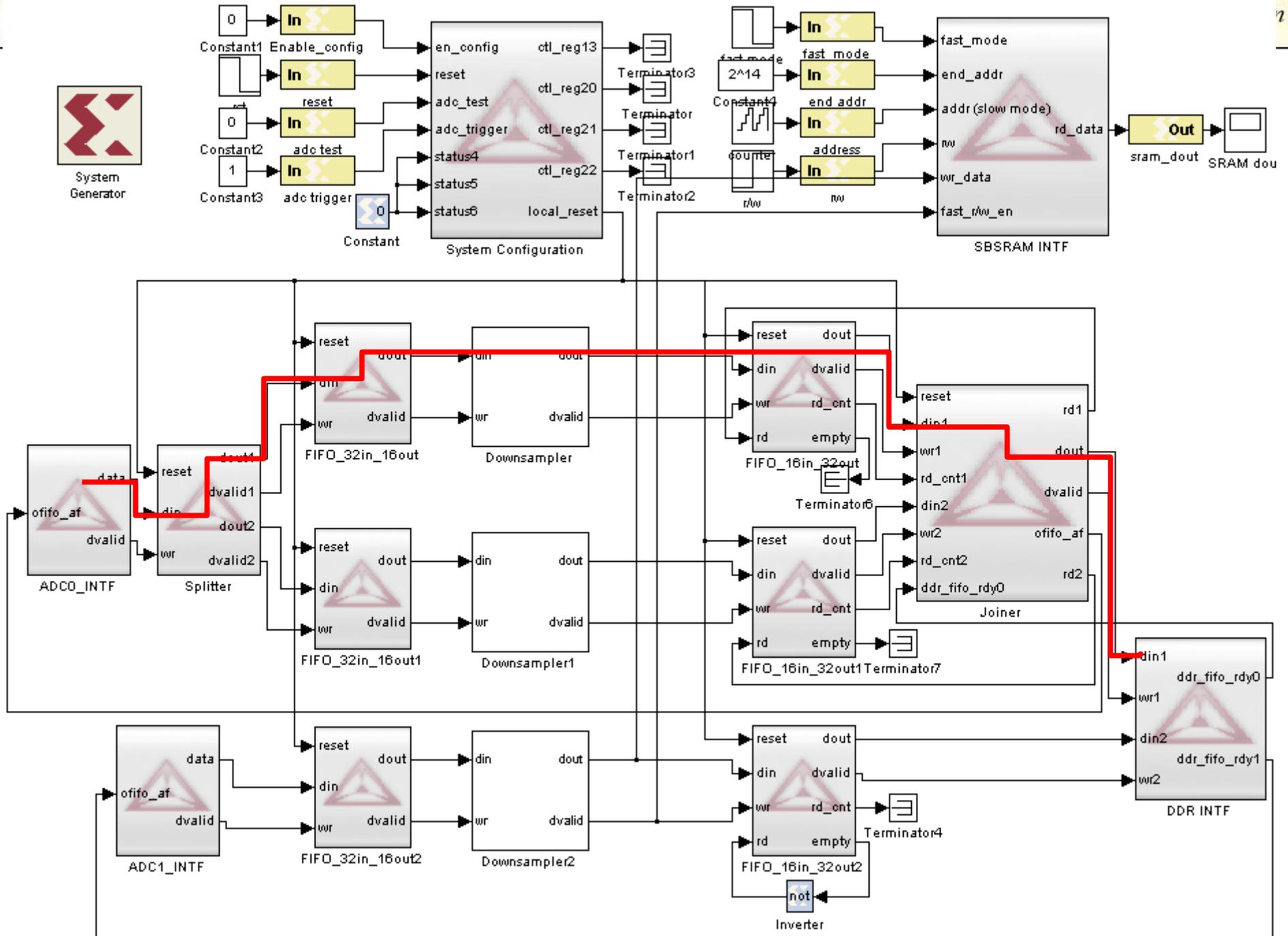
- System Configuration:** en_config, reset, adc_test, adc_trigger, status4, status5, status6, ctl_reg13, ctl_reg20, ctl_reg21, ctl_reg22, local_reset
- ADC0_INTF:** data, ofifo_af, dvalid
- ADC1_INTF:** data, ofifo_af, dvalid
- DDR INTF:** din1, wr1, din2, wr2, ddr_fifo_rdy0, ddr_fifo_rdy1
- SBSRAM INTF:** fast_mode, end_addr, addr (slow mode), rd_data, wr_data, fast_rw_en
- FIFO_32in_16out:** reset, din, wr, dout, dvalid
- Splitter:** reset, din, wr, dout1, dvalid1, dout2, dvalid2
- FIFO_16in_32out:** reset, din, wr, rd, rd_cnt, empty
- Joiner:** reset, din1, wr1, rd_cnt1, din2, wr2, rd_cnt2, ddr_fifo_rdy0, rd1, dout, dvalid, ofifo_af, rd2

Compilation Flow

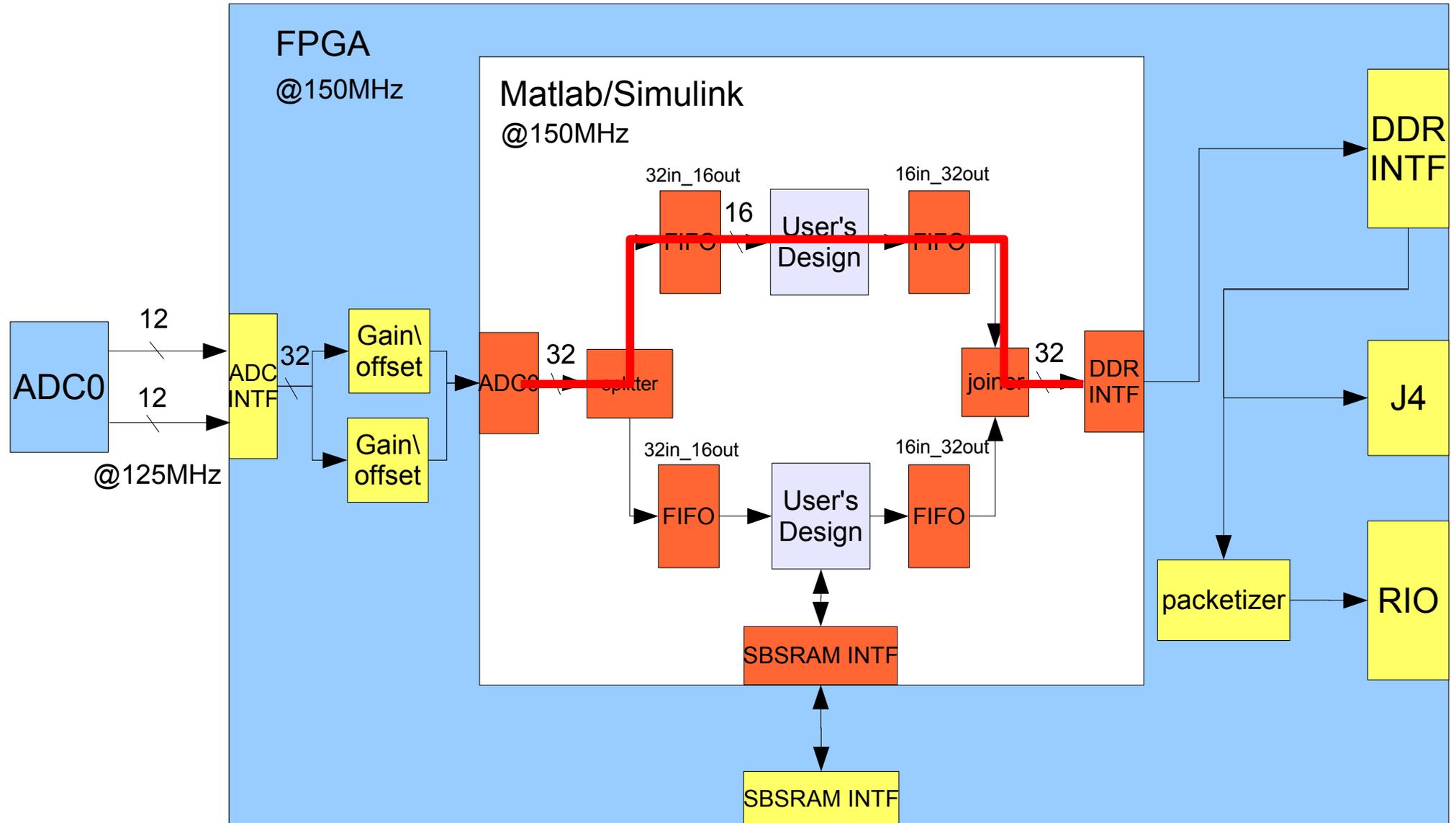


Demo

Build Your Design

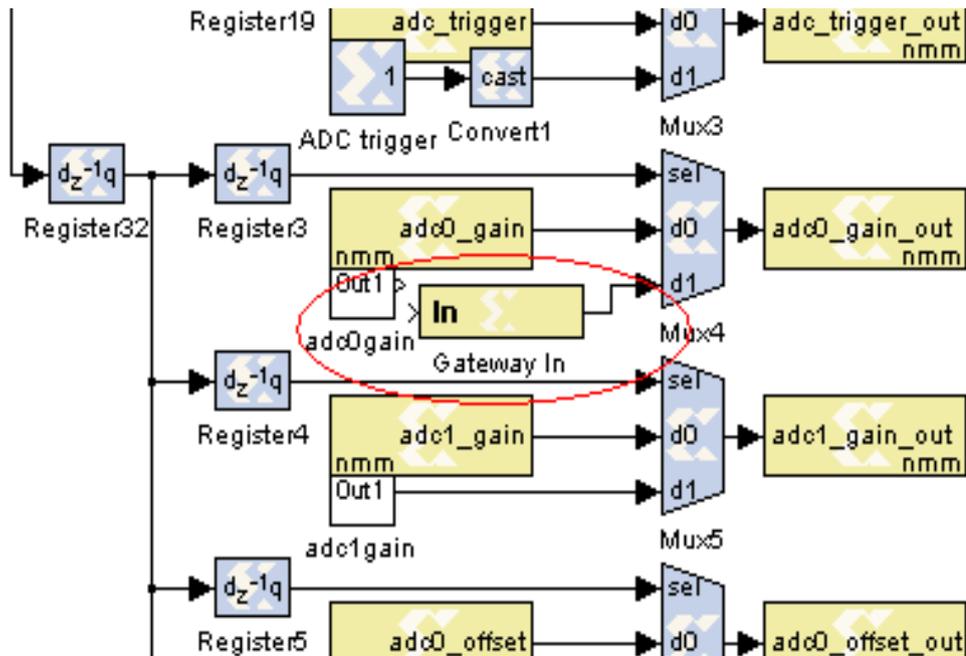


PMC UWB Block Diagram



NEW Feature – System Configuration Panel

- Easy configuration
- No software needed
- Capability of changing settings on the fly



Function Block Parameters: System Configuration

UWB Simulink Block (mask)

This block sets up the command registers in Matlab. When "Enable Configuration" is '1', all parameters are provided by Matlab. When "Enable Configuration" is '0', the parameters are from the host. Four 32 bit host controlled registers 13, 20, 21, and 22 can be monitored inside Matlab. Three 32 bit status ports provide information of user's design to the host. Please refer to Registers section in FrameWork Logic User Guide for more information.

Parameters

Run

ADC0 Channel Enable

ADC0 Clock Select: PLL

ADC0 Desinations: PCI

ADC0 Gain (0 - 2): 1

ADC0 Offset ($2^0 - 2^{15}$): 0

ADC1 Channel Enable

ADC1 Clock Select: PLL

ADC1 Desinations: PCI

ADC1 Gain (0 - 2): 1

ADC1 Offset ($2^0 - 2^{15}$): 0

Bypass VCO

Xtal Sel: Xtal

PLL Feedback Divider Ratio M (1 - 512): 28

PLL Output Divider Ratio N: N=4

Sync Clock Select: ACLK

Divider Clock Select: ACLK

Divider Ratio: D=1

OK

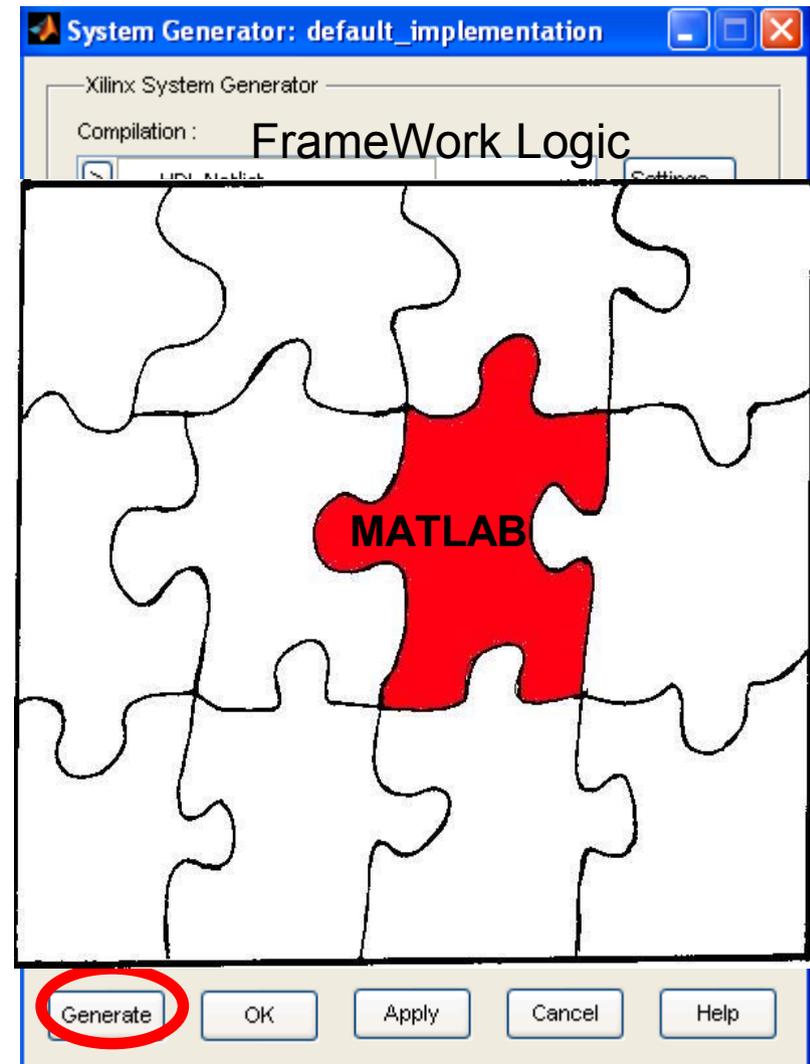
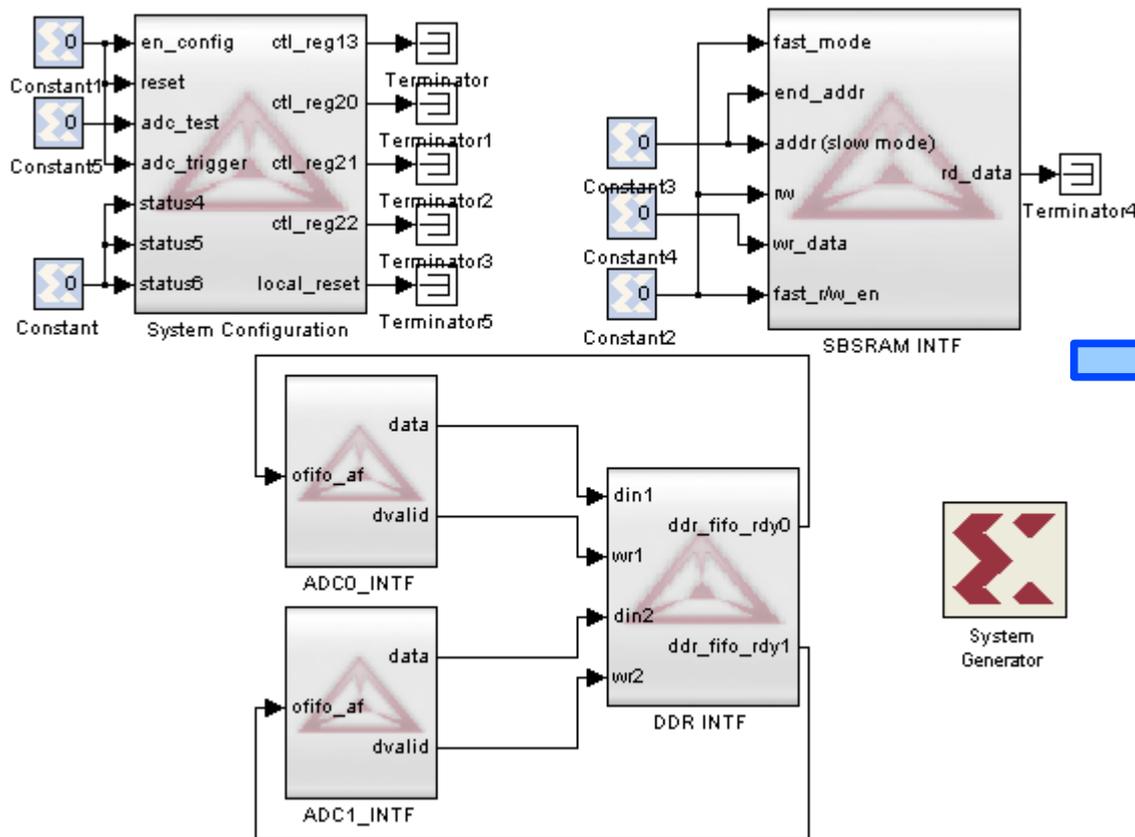
Cancel

Help

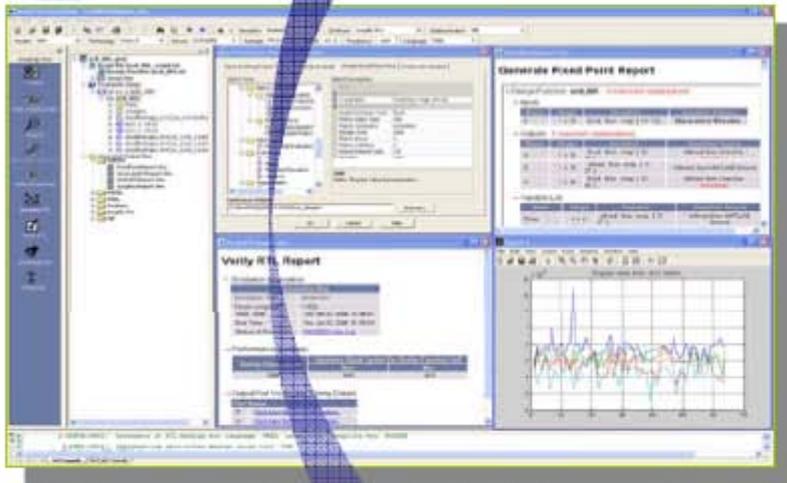
Apply

Integrating MATLAB Core into FrameWork Logic

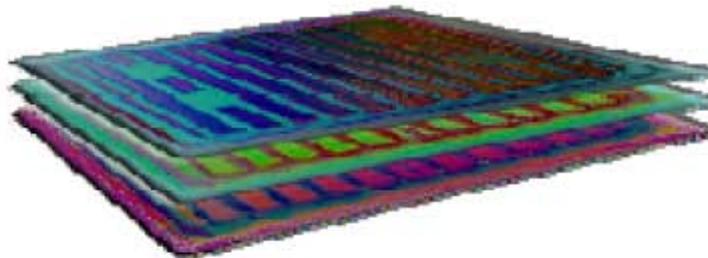
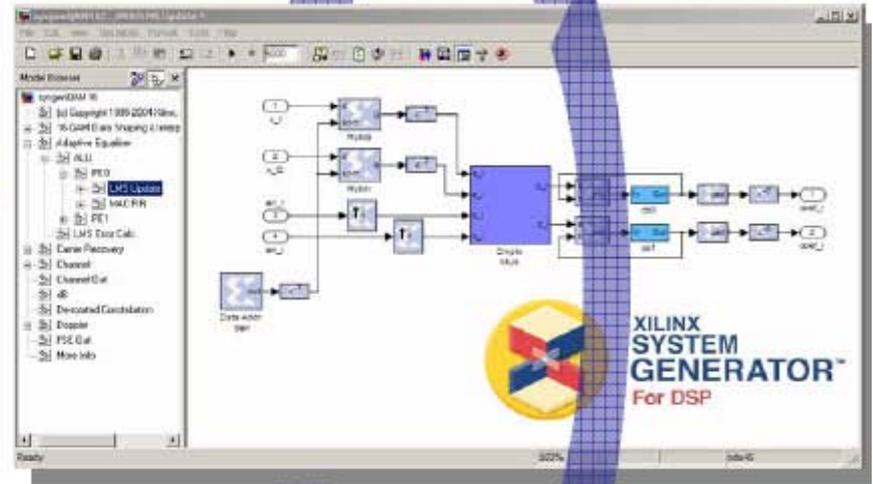
Replace Gateways with constants
for final implementation



Design in MATLAB/Simulink



Generate



FrameWork VHDL Logic Design

II Framework Logic



- Framework Logic Features
 - Comprehensive board support packages in MATLAB and VHDL for FPGA signal processing development
 - Hardware interface layer design structure allows rapid integration of application specific code
 - Designed to support real time signal processing and data acquisition
 - Complete end-to-end simulation testbench using ModelSim
 - Reference designs illustrating hardware use
 - Saves time by providing a simplified access to the hardware and data stream
 - Supported by software for control, data logging and signal generation
 - Get you off to a quick start
- *Reduced design, test and verification time*

Innovative IP Core Library



Hardware Control Cores	Function
Virtual FIFO	Implements a FIFO using DDR DRAM memory buffer
Multi-queue FIFO	Implements multiple FIFO queues in DDR DRAM memory buffer
Pattern Generator	Implements a dynamically loadable pattern generator for DDR DRAM capable of >500 MB/s sustained operation
SRAM Controller	Provides high speed synchronous SRAM interface
Packetizer	Packetizes data for system interfaces
Deframer	Unpacketizes data from system interface
J4 Link	Implements a data link over PMC J4 connection to base cards capable of >350 MB/s
SFP Data link	Provides an SFP data link interface (Quadia)
RIO Data Link	Provides a RIO link interface between FPGAs with flow control
DSP interfaces	Interface cores for standard TI DSPs ('6416, '6713)
DDC Interface	Interface to TI GC5016 quad-channel DDC devices
Quadrature Decoding	Interface to industry-standard quadrature encoders
Sigma Delta DAC	Sigma Delta modulator and controls implements a DAC function. External analog filter is required.
Triggering Controls	Snapshots, external triggering, decimation

DSP Cores	Function
Digital Downconversion	20 channels DDC operating at up to 208 MHz
Spectral Inverter	Real-time spectral inversion
FFT	Radix-2 FFT, 32 to 8K record lengths
FIR Filters	Support via Xilinx Corelib and Matlab. The number of taps that may be implement for real time operation depends on sample rate, logic utilization and logic clock rate.
CIC Filters	Support via Xilinx Corelib and Matlab.

Xilinx IP Cores

Xilinx CORE Generator - E:\coregen\coregen\DR\coregen\cor...

File Project Tools Help

Show Latest Versions

Function	Version	License
Automotive & Industrial		
Basic Elements		
Communication & Networking		
Building Blocks		
Error Correction		
Ethernet		
LVDS		
Modulation		
Networking		
Serial Interfaces		
Telecommunications		
Digital Signal Processing		
Building Blocks		
Correlators		
Filters		
Cascaded Integrator Comb Filter	3.0	
Distributed Arithmetic FIR Filter	9.0	
FIR Compiler	3.0	
MAC FIR Filter	5.1	
Modulation		
Multiply Accumulators		
Transforms		
Trig Functions		
Waveform Synthesis		
FPGA Features and Design		
Math Functions		
Memories & Storage Elements		
Standard Bus Interfaces		
Storage, NAS and SAN		

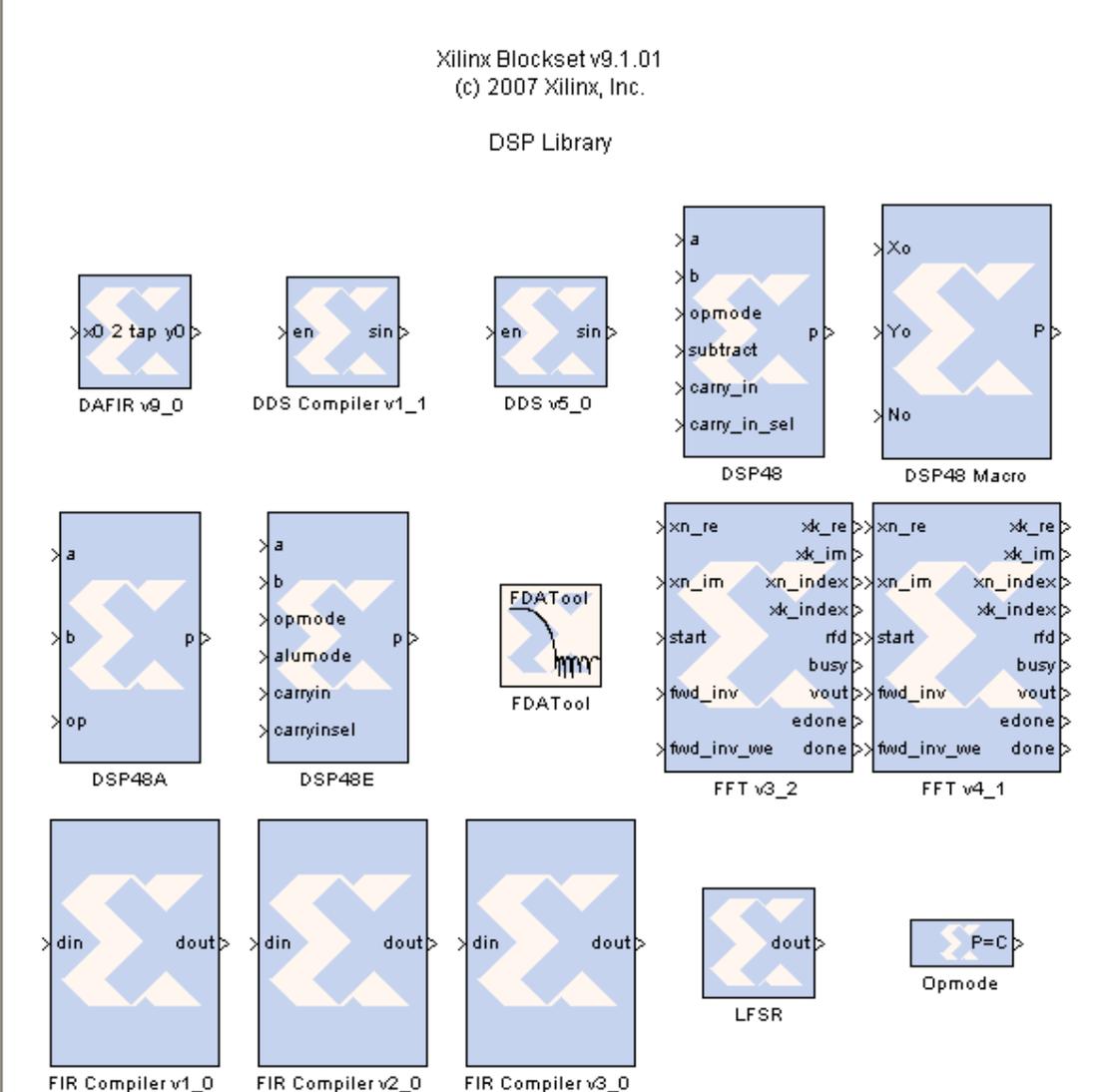
View by Function | View by Name | Generated IP

Library: xbsDSP_r4

File Edit View Format Help

Xilinx Blockset v9.1.01
(c) 2007 Xilinx, Inc.

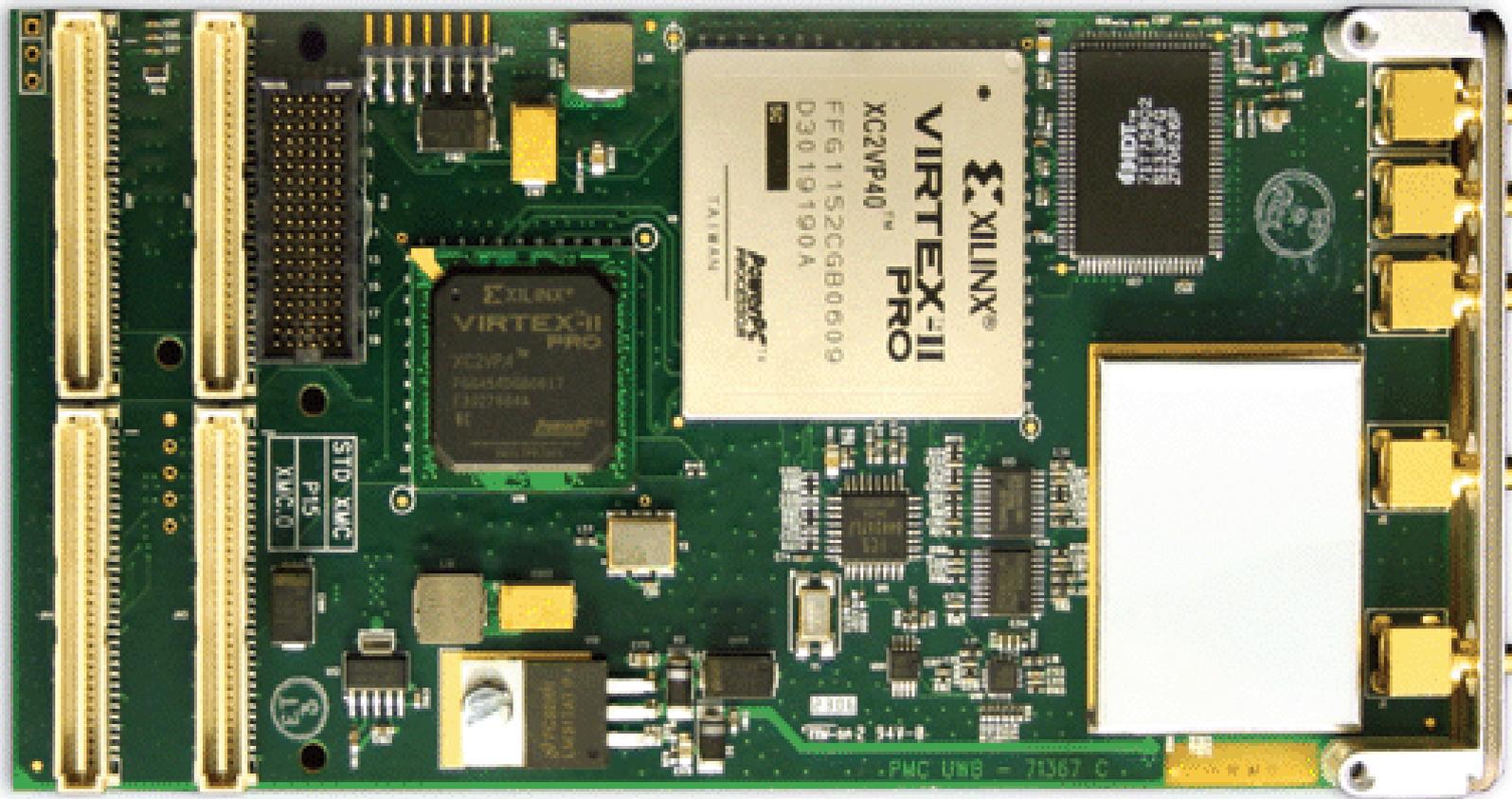
DSP Library



Ready | 100% | Locked

Example: FIR Filter in UWB

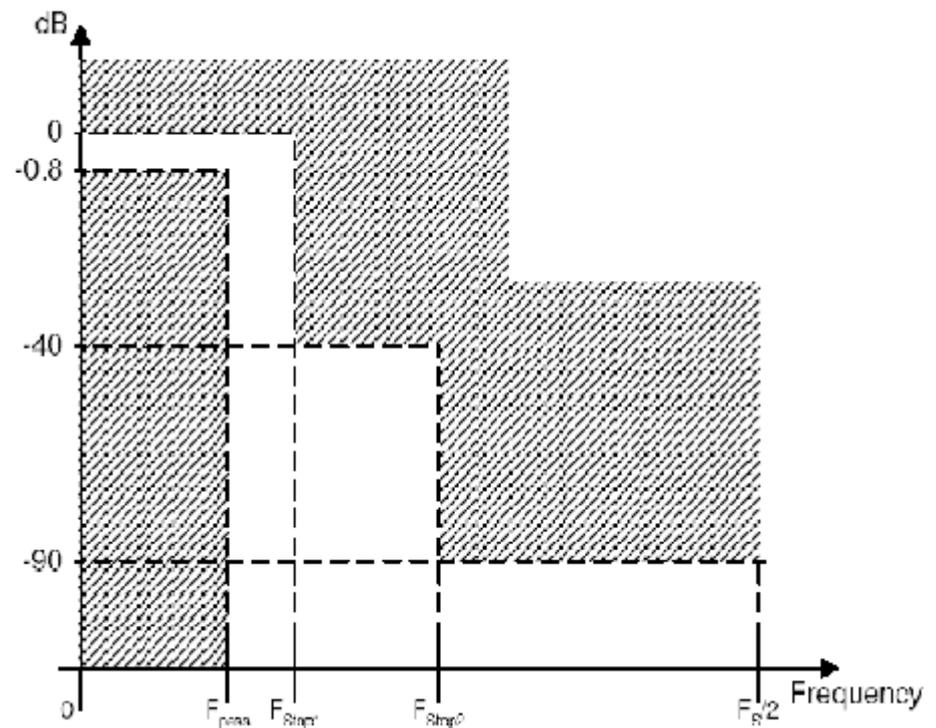
- Two 12-bit 250 MSPS AD converters
- Virtex-II Pro FPGA, 4 Million gates
- 64MB SDRAM plus 2MB SRAM for FPGA
- Sample clocks: dual external or on-board PLL
- Software Defined Radio (SDR)
- Electronic Warfare
- Advanced RADAR
- Telecom IP development



VHDL Design Flow

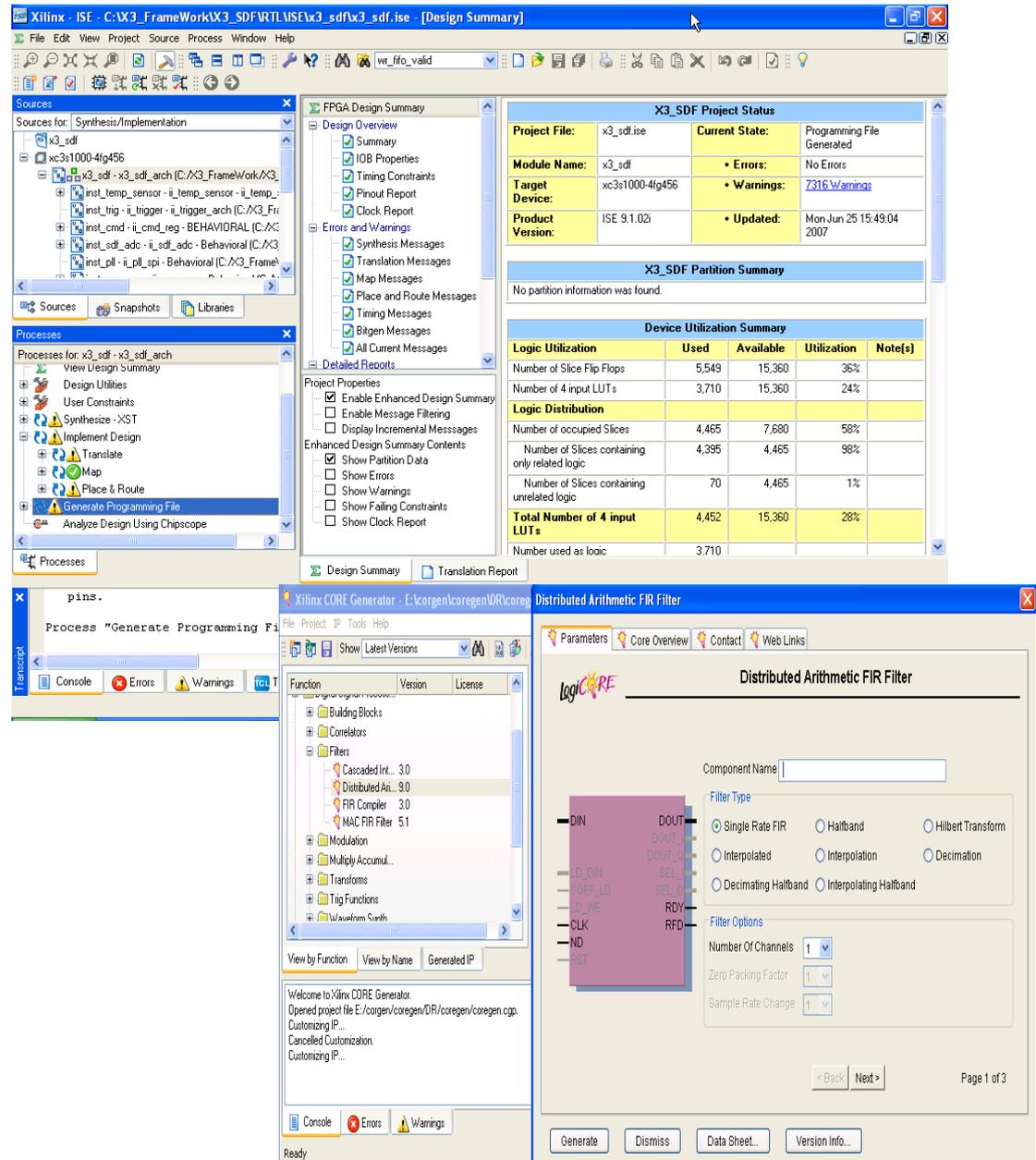
Step 1 : Define system requirements and architecture

- Define DSP, data analysis, triggering and system control functions
- Define accuracy and dynamic range requirements
- Identify real-time constraints such as data rates and processing rates
- Identify system data buffering requirements
- Estimate logic usage



Step 2 – Create cores and logic

- Create new logic and cores using Xilinx Core Generator, MATLAB, or VHDL
- Simulate and verify core functionality



The screenshot displays the Xilinx ISE Design Summary window and the Xilinx CORE Generator interface. The Design Summary window shows the project status, partition summary, and device utilization summary. The CORE Generator interface shows the Distributed Arithmetic FIR Filter core configuration.

X3_SDF Project Status

Project File:	x3_sdf.isc	Current State:	Programming File Generated
Module Name:	x3_sdf	• Errors:	No Errors
Target Device:	xc3s1000-4fg456	• Warnings:	7316 Warnings
Product Version:	ISE 9.1.02i	• Updated:	Mon Jun 25 15:49:04 2007

X3_SDF Partition Summary

No partition information was found.

Device Utilization Summary

Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Flip Flops	5,549	15,360	36%	
Number of 4 input LUTs	3,710	15,360	24%	
Logic Distribution				
Number of occupied Slices	4,465	7,680	58%	
Number of Slices containing only related logic	4,395	4,465	98%	
Number of Slices containing unrelated logic	70	4,465	1%	
Total Number of 4 input LUTs	4,452	15,360	28%	
Number used as logic	3,710			

Xilinx CORE Generator - Distributed Arithmetic FIR Filter

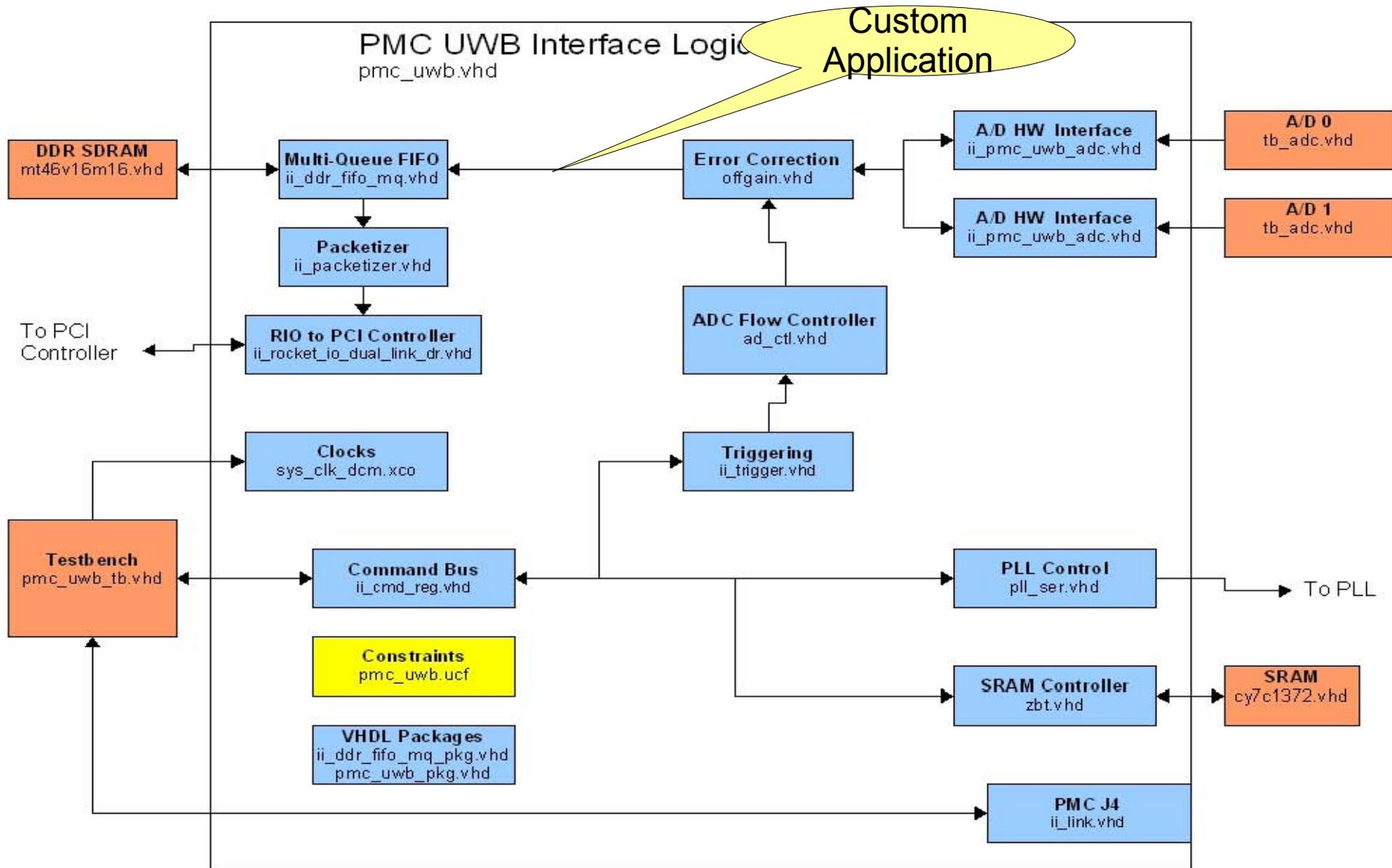
Function: DistributedAri... Version: 3.0 License: ...

Filter Type: Single Rate FIR Halfband Hilbert Transform
 Interpolated Interpolation Decimation
 Decimating Halfband Interpolating Halfband

Filter Options: Number of Channels: 1, Zero Packing Factor: 1, Sample Rate Change: 1

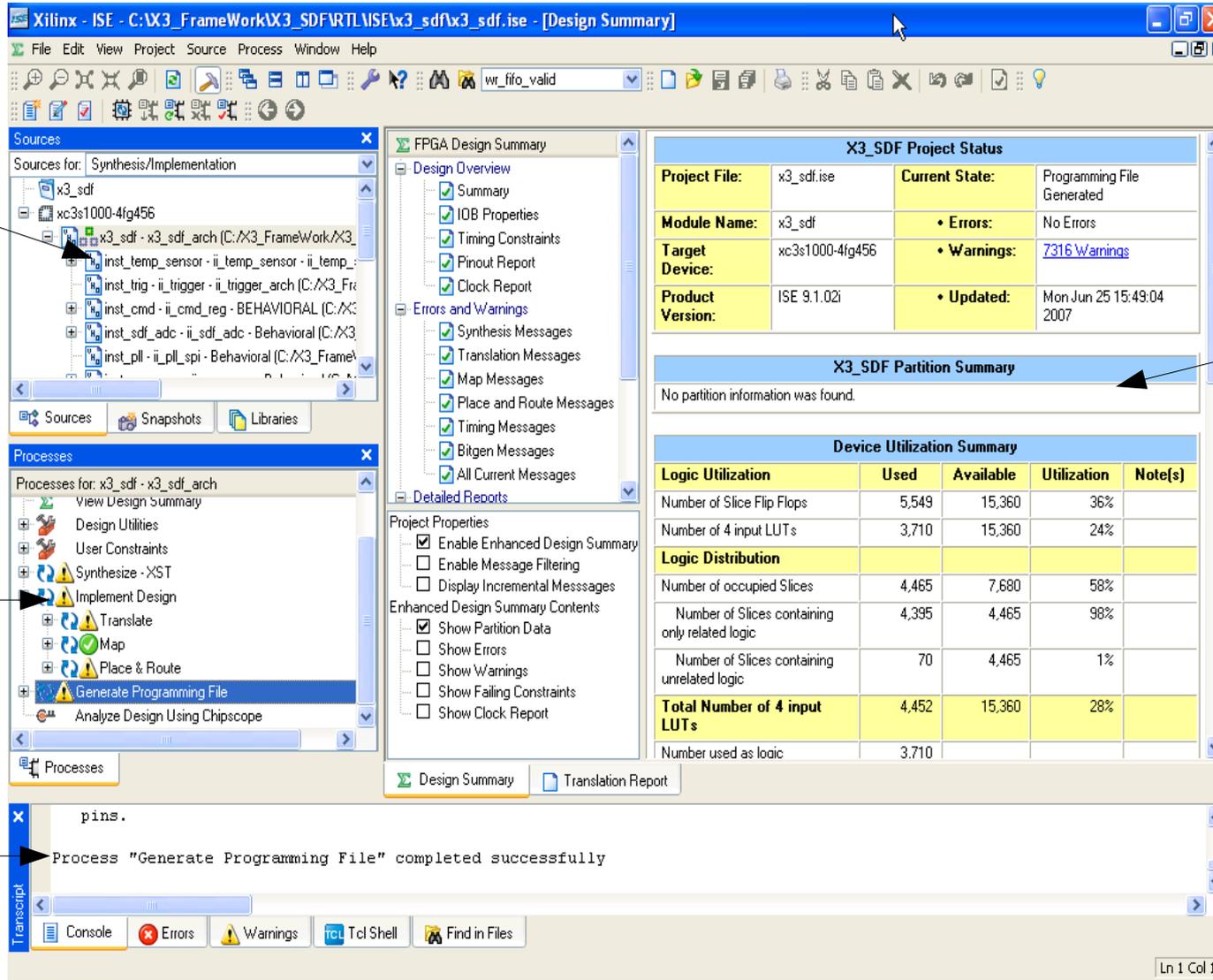
Buttons: Generate, Dismiss, Data Sheet..., Version Info...

Step 3 – Add functions to Framework Logic



Xilinx ISE Environment

Sources



The screenshot shows the Xilinx ISE Design Summary window. The 'Sources' pane on the left lists project files for synthesis/implementation, including xc3s1000-4fg456 and various behavioral models. The 'Processes' pane shows the 'Generate Programming File' process as the current step. The 'FPGA Design Summary' pane is expanded to show 'Errors and Warnings', which includes synthesis, translation, and timing messages. The 'X3_SDF Project Status' table provides key project information. The 'X3_SDF Partition Summary' table shows no partition information. The 'Device Utilization Summary' table details logic utilization and distribution. The 'Console' pane at the bottom shows the successful completion of the 'Generate Programming File' process.

Project File:	x3_sdf.isc	Current State:	Programming File Generated
Module Name:	x3_sdf	• Errors:	No Errors
Target Device:	xc3s1000-4fg456	• Warnings:	7316 Warnings
Product Version:	ISE 9.1.02i	• Updated:	Mon Jun 25 15:49:04 2007

No partition information was found.			
-------------------------------------	--	--	--

Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Flip Flops	5,549	15,360	36%	
Number of 4 input LUTs	3,710	15,360	24%	
Logic Distribution				
Number of occupied Slices	4,465	7,680	58%	
Number of Slices containing only related logic	4,395	4,465	98%	
Number of Slices containing unrelated logic	70	4,465	1%	
Total Number of 4 input LUTs	4,452	15,360	28%	
Number used as logic	3,710			

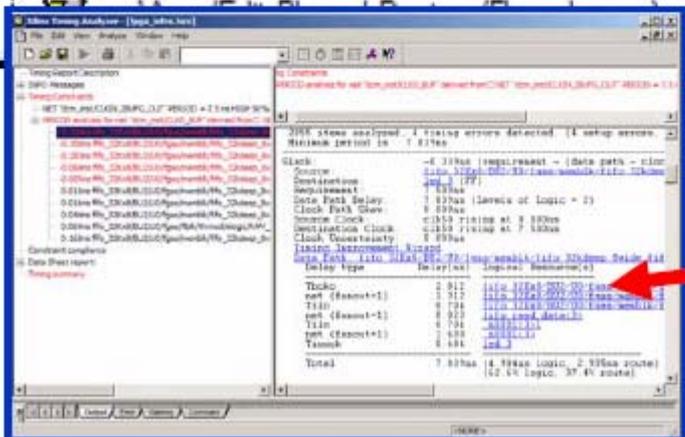
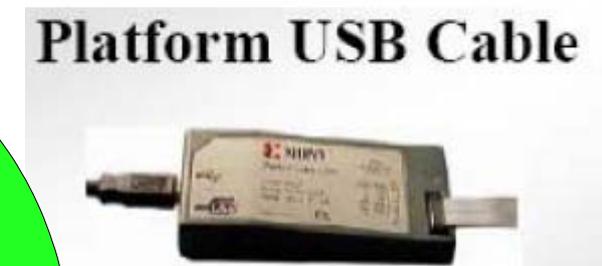
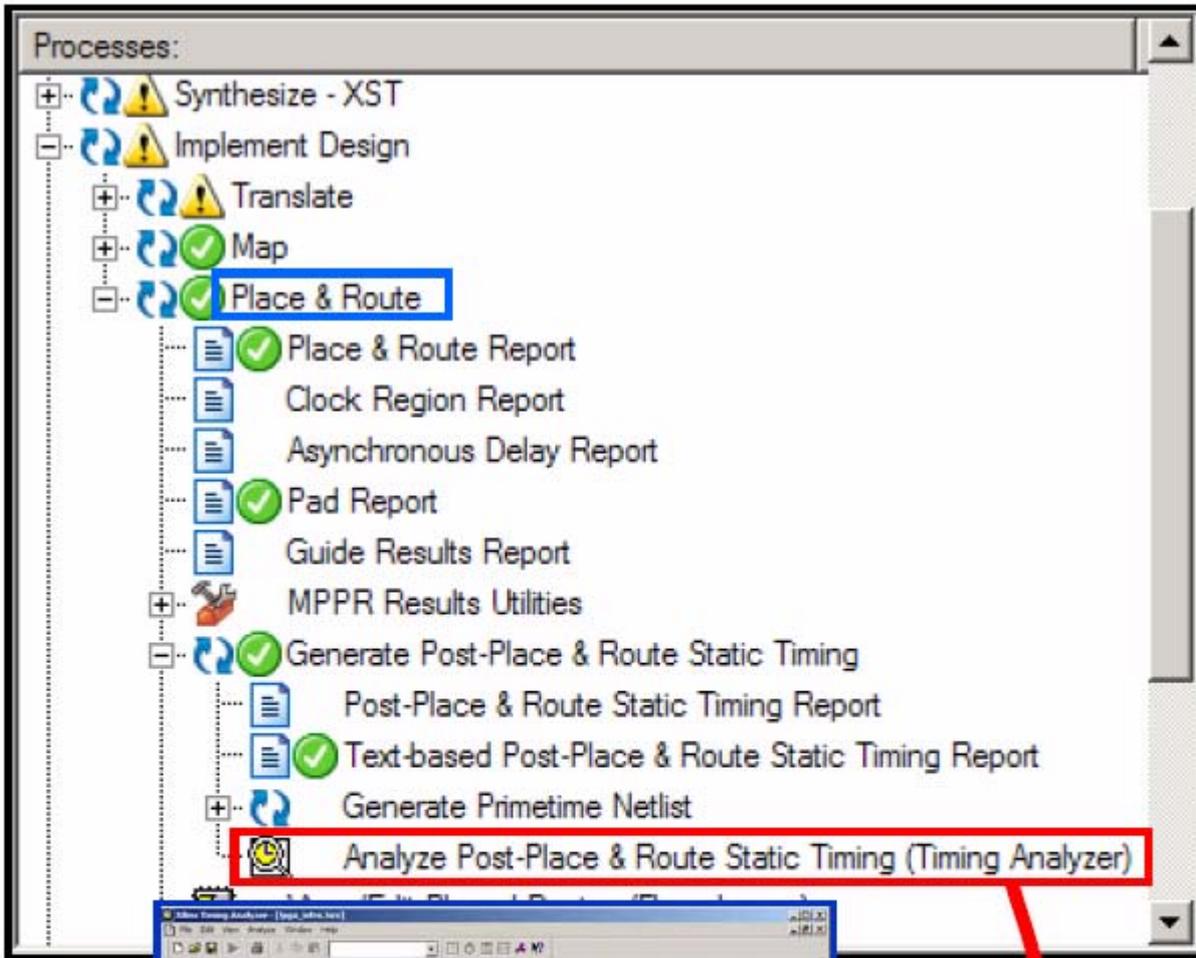
```
pins.  
Process "Generate Programming File" completed successfully
```

Processes

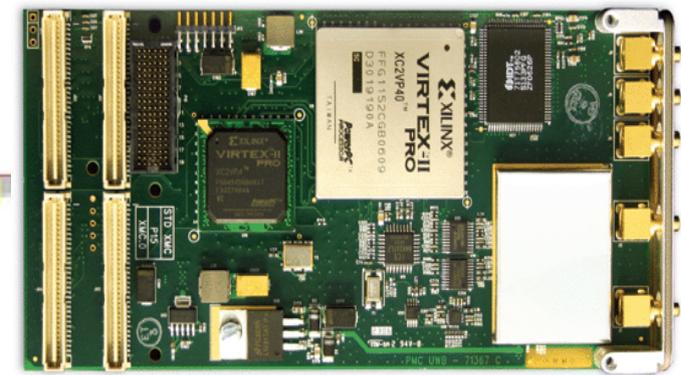
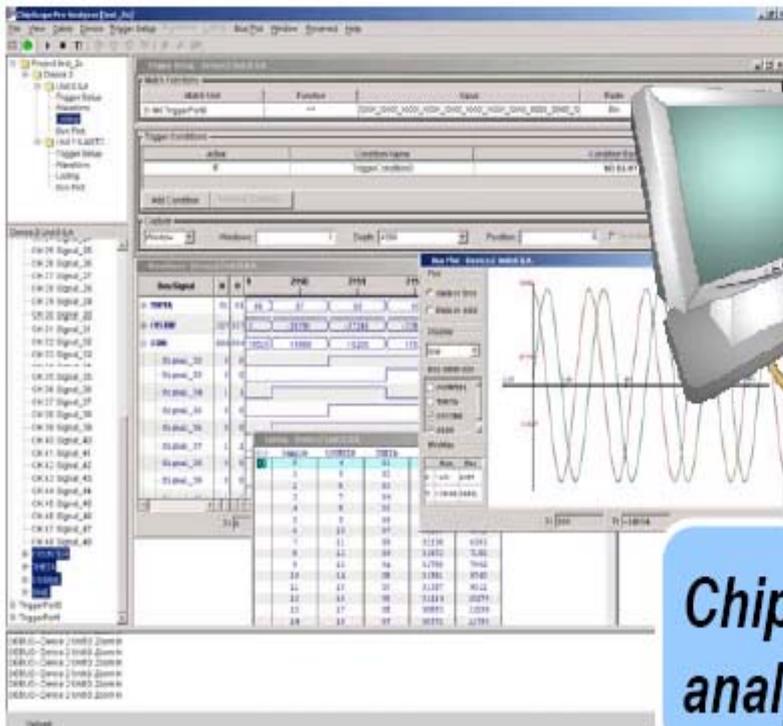
Project Summary

Console

Step 5: Compile and Download Logic



Step 6 - Debug

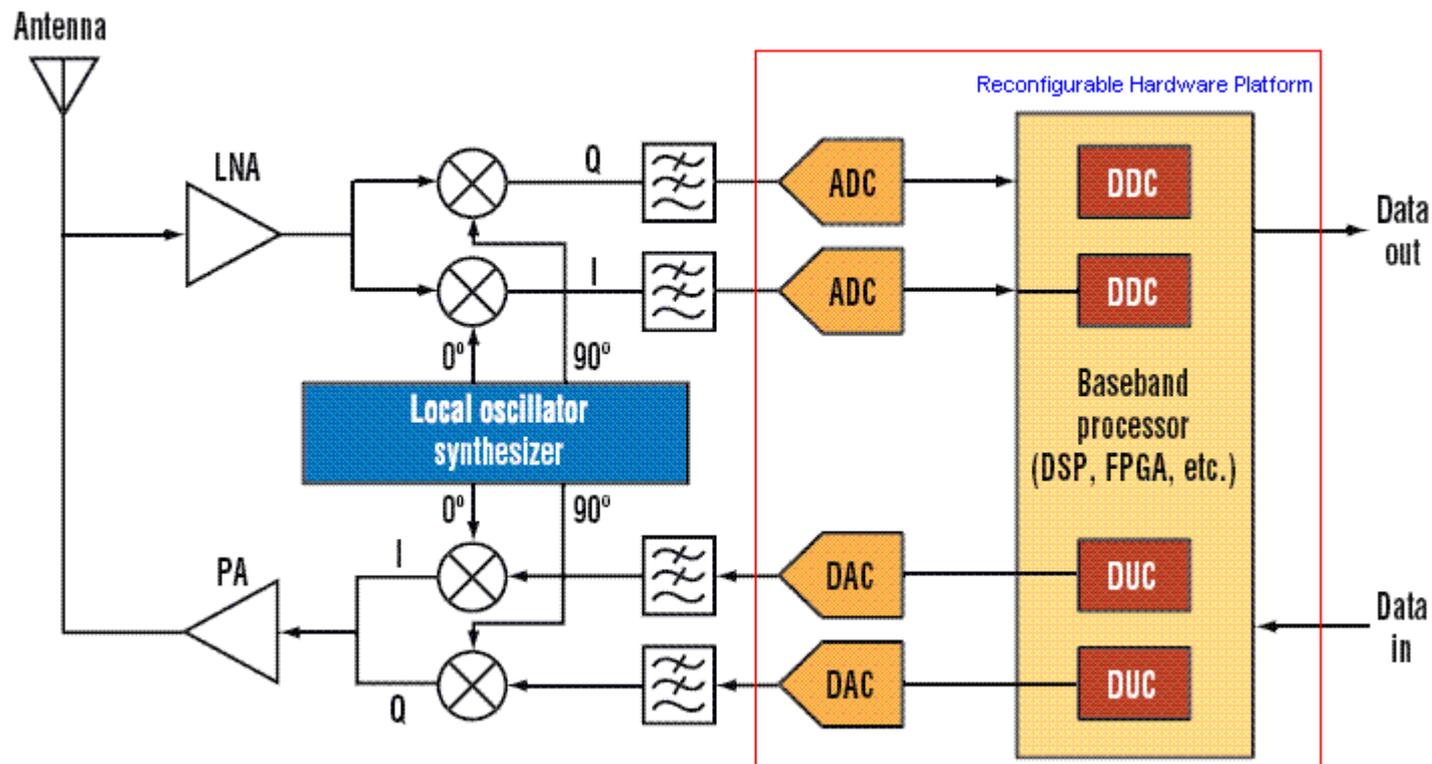


ChipScope Pro Analyzer functions as a logic analyzer, bus analyzer, and control console

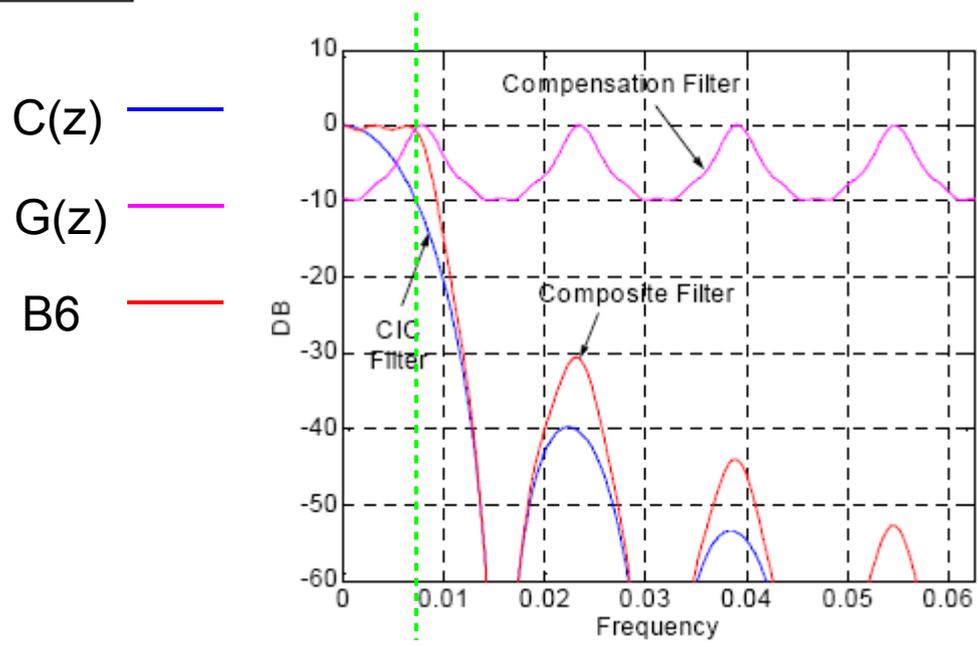
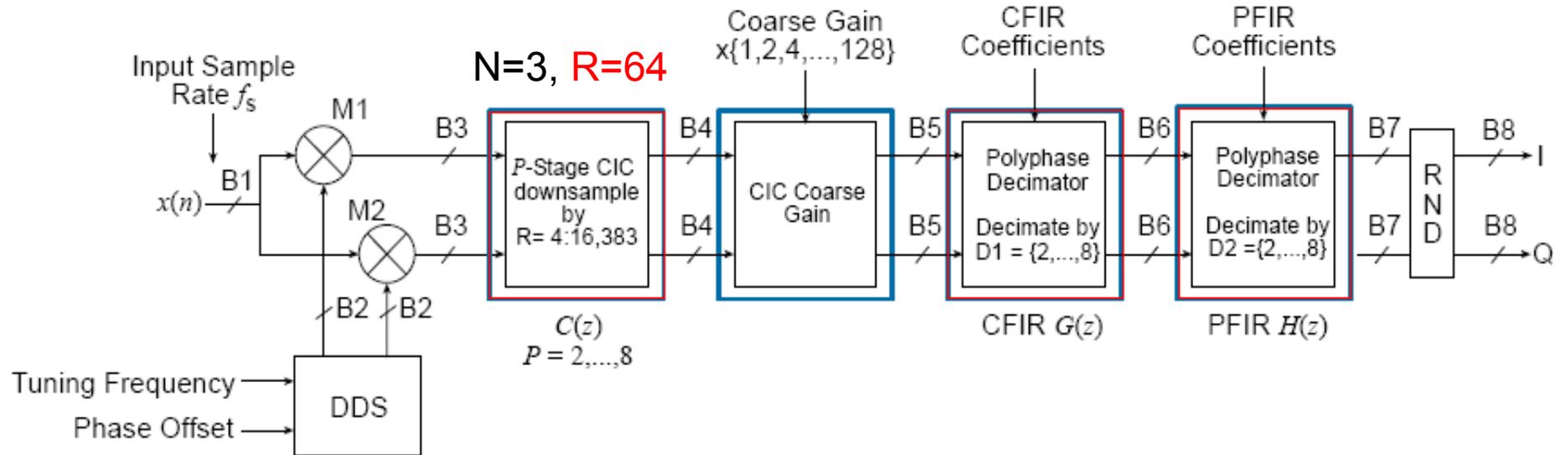
Software Defined Radio

Software Defined Radio

- Wireless communication issue today
 - Compatibility & Spectrum usage
- Purpose
 - Produce a radio that can receive and transmit a new form of radio protocol by running new software
- Key
 - Software- programmable hardware



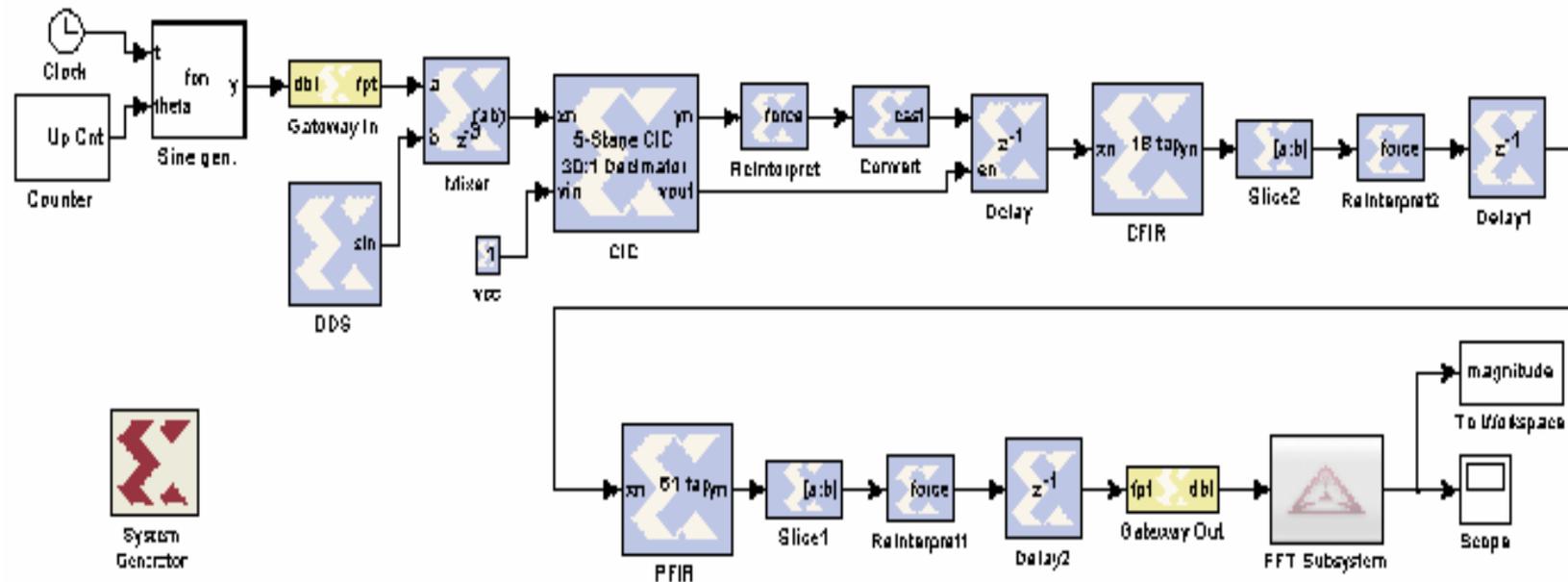
Digital Down Converter (DDC)



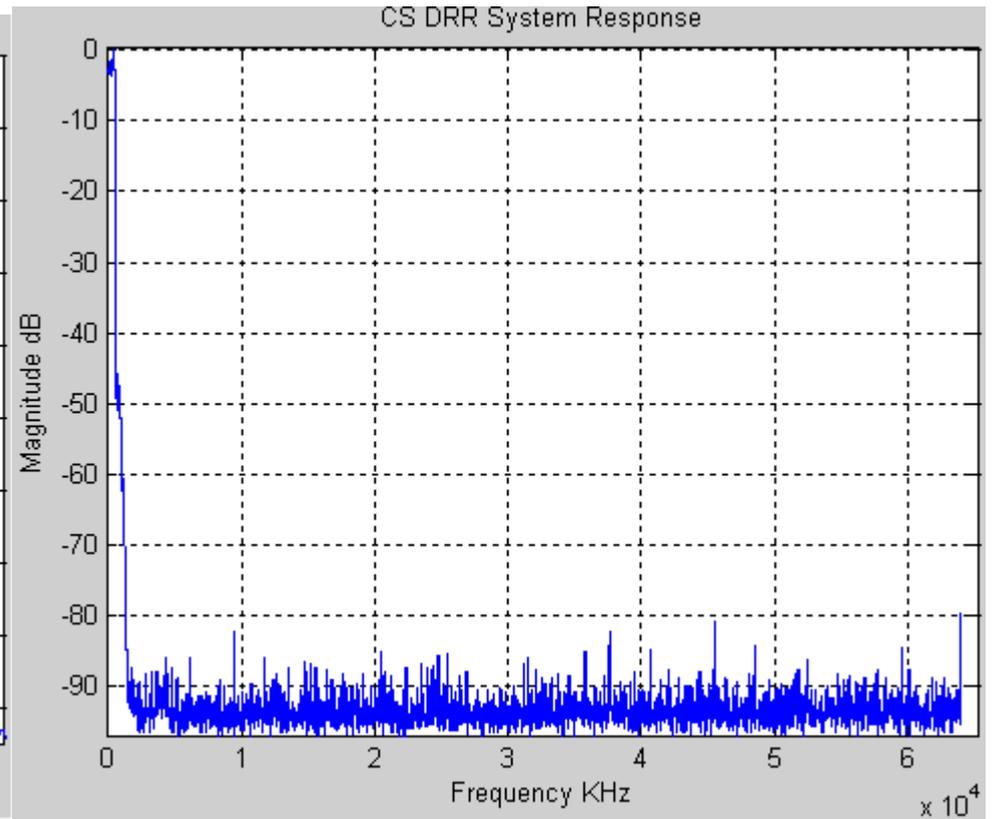
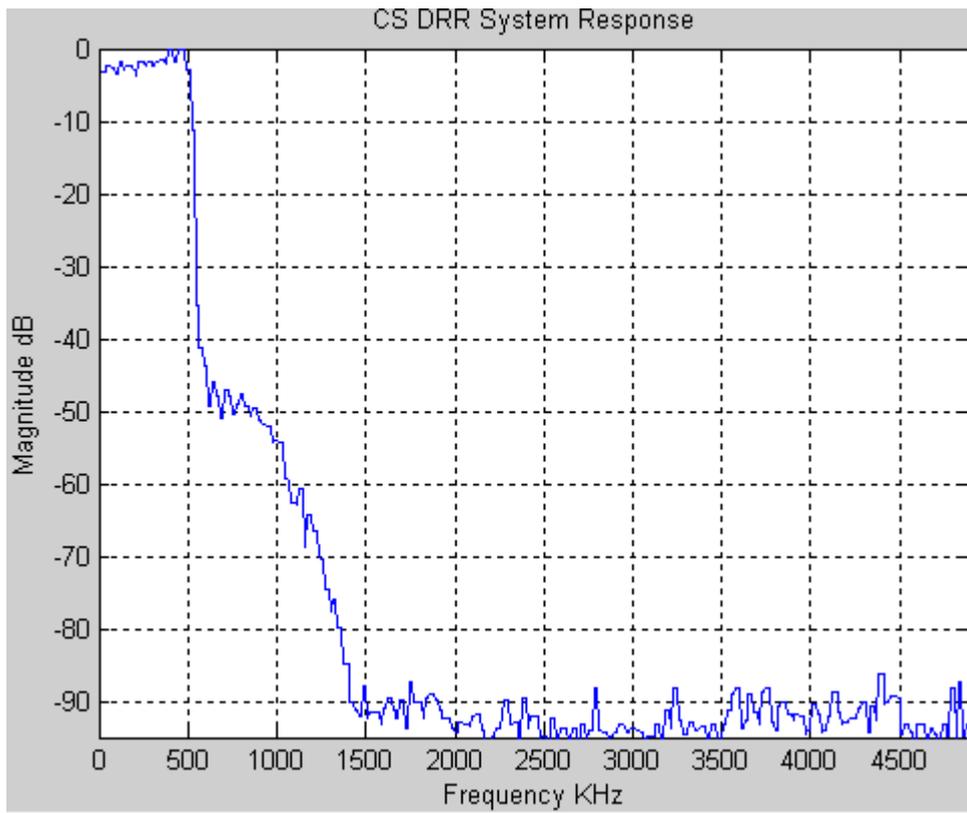
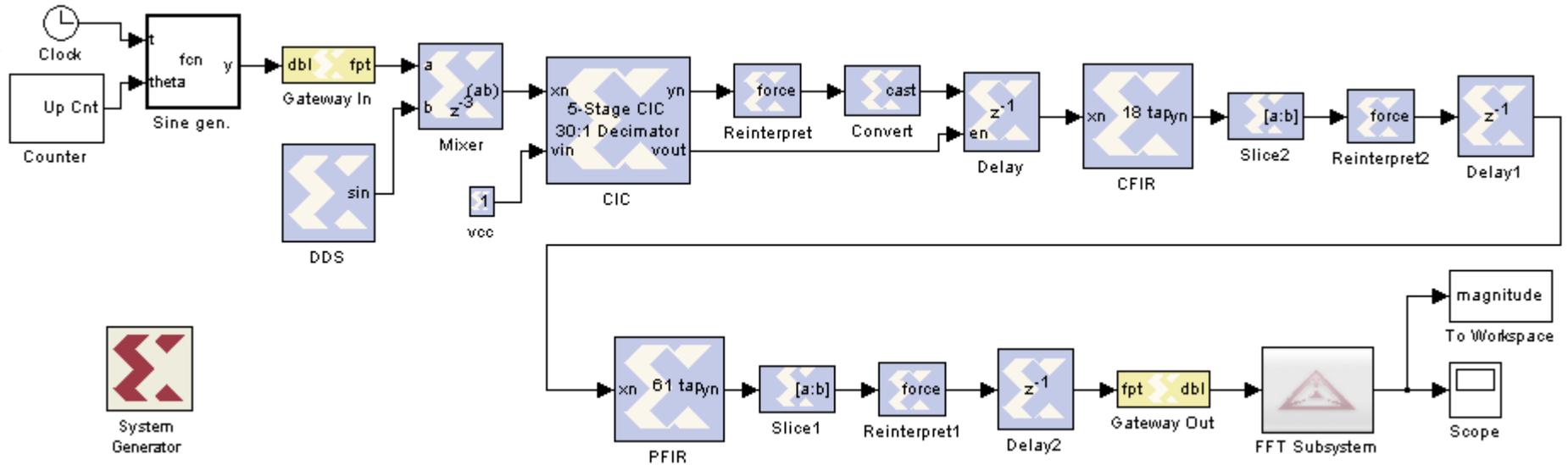
Normalized freq
 $0.5 / 64 = 0.0078$

Our DDC Solution

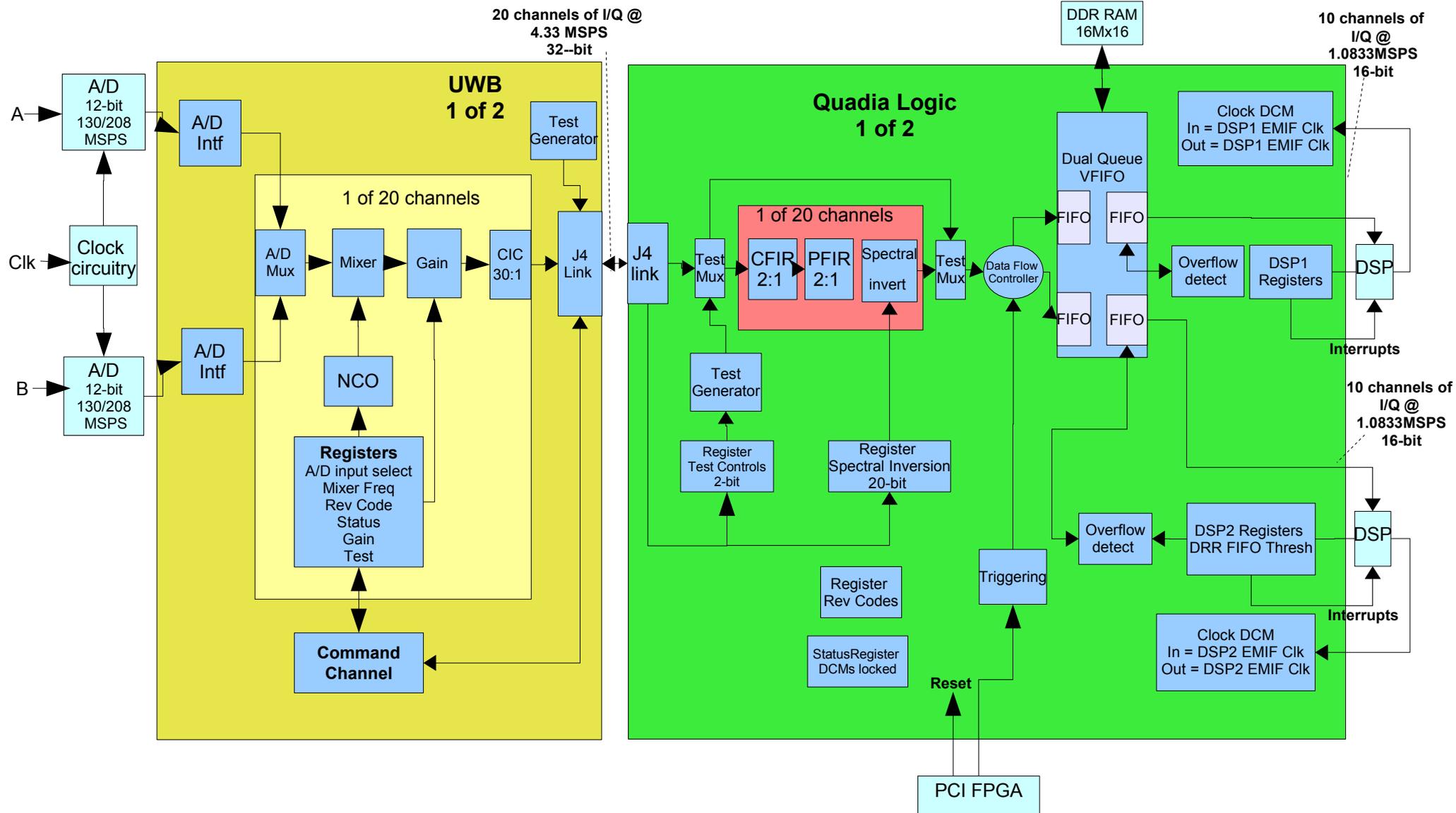
- MATLAB Simulink design for FPGA
- Supports up to 208 MSPS with >90 dB dynamic range
- 10 kHz tuning resolution



MATLAB Simulation (Bit True, Cycle True)

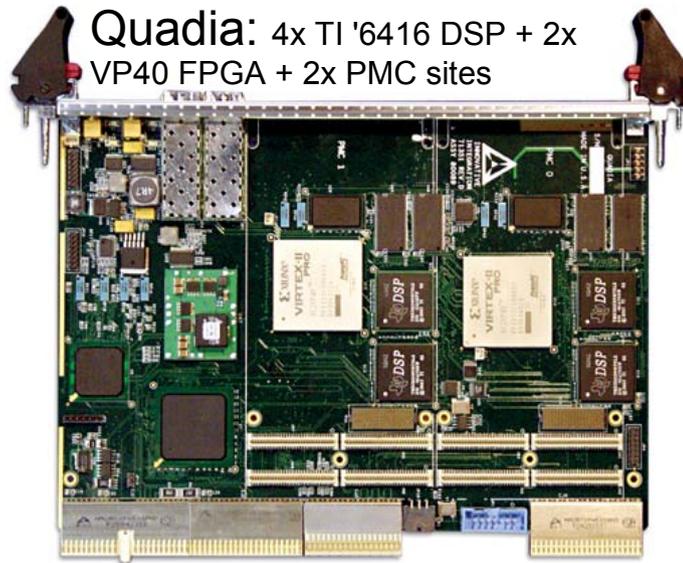


II Digital Receiver (SDR)

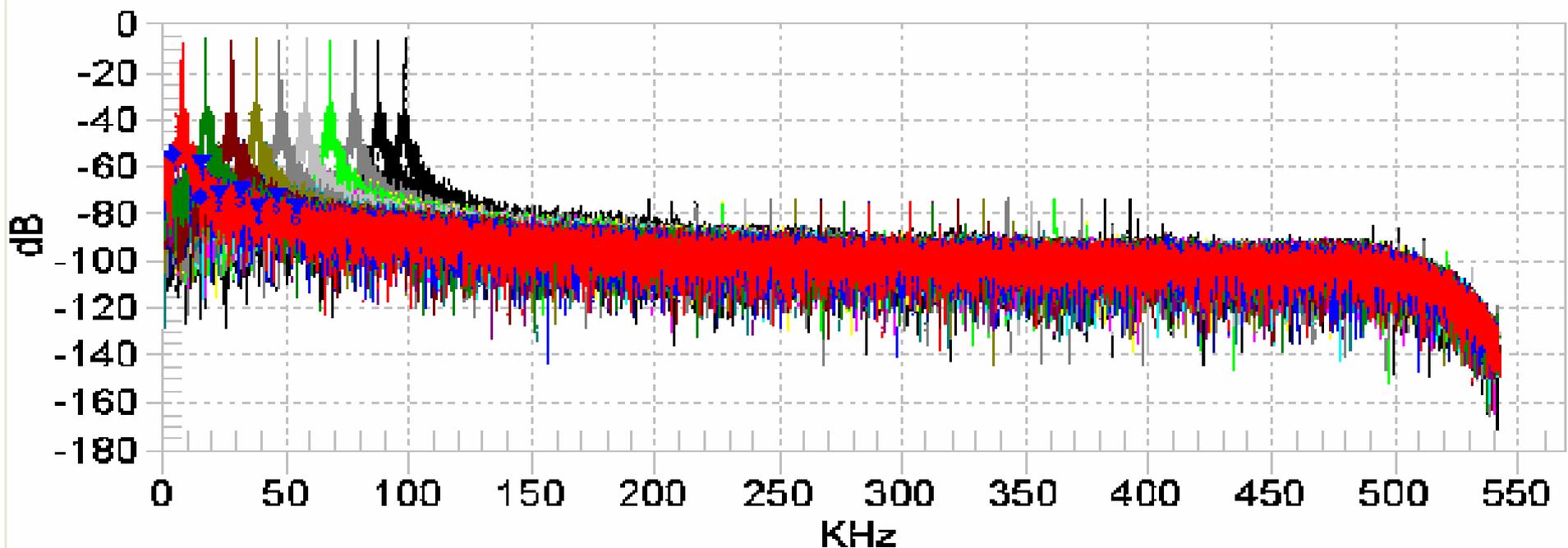


Software Defined Radio Results

- SDR implemented on Quadia and UWB
- Example results shown for 97.5MHz input, 130 MSPS sampling, channels tuned to $97.5+n*10\text{KHz}$



PMC UWB:
2x 250 MSPS A/D
+ VP40 FPGA



II SDR Support



- Logic designs and supporting software are available for application development
- Full application note available

