

X3-10M

v1.2



PCI Express XMC Module with 8 simultaneous channels of 25 MSPS 16-bit A/D, and 1.8M FPGA with DSP

FEATURES

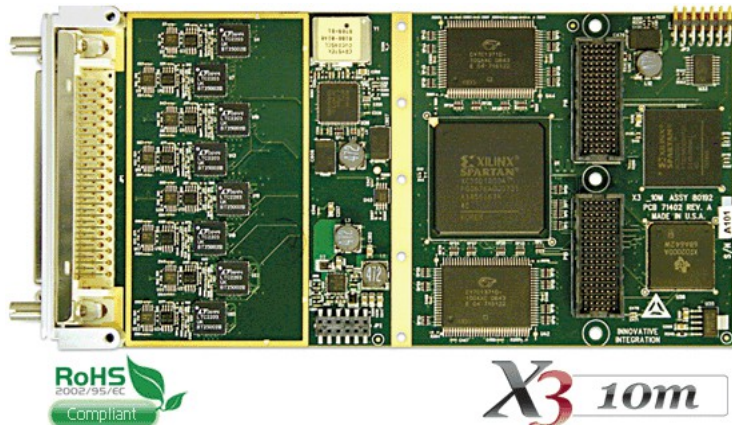
- 8 channels of 25 MSPS, 16-bit simultaneously sampling A/D
- -110 dB noise floor, 97 dB SFDR
- Snap any channel pair at up to 20 MSPS per channel
- Continuously acquire 8 simultaneous channels at 10 MSPS to system memory
- Programmable input ranges: +/-2V, +/-1V, +/-0.4V, +/-0.2V
- High impedance, differential inputs
- Xilinx Spartan3A DSP, 1.8M gate FPGA
- 4MB SRAM
- Sample clock is external or programmable low jitter PLL
- Framed, software or external triggering
- Log acquisition timing and events
- 44 bits digital IO on P16
- Power Management features
- PCI Express XMC Module (75x150 mm)
- Use in any PCI Express desktop, compact PCI/PXI, or cabled PCI Express application

APPLICATIONS

- Multichannel sensor interface
- Neuro-physical instrumentation
- RADAR

SOFTWARE

- Data Acquisition, Logging and Analysis applications provided
- Windows/Linux Drivers
- C++ Host Tools
- VHDL/MATLAB Logic Tools



DESCRIPTION

The X3-10M is an XMC IO module featuring eight simultaneously sampling 16-bit, 25 MSPS A/D channels designed for high speed instrumentation and analysis for neuro-physical, RADAR, and high speed data acquisition applications.

Flexible trigger methods include counted frames, software triggering and external triggering. The sample rate clock is either an external clock or on-board programmable PLL clock source.

Data acquisition control, signal processing, buffering, and system interface functions are implemented in a Xilinx Spartan3A DSP FPGA, 1.8M gate device. Two 512Kx32 memory devices are used for data buffering and FPGA computing memory.

The logic can be fully customized using VHDL and MATLAB using the FrameWork Logic toolset. The MATLAB BSP supports real-time hardware-in-the-loop development using the graphical, block diagram Simulink environment with Xilinx System Generator.

The PCI Express interface supports continuous data rates up to 180 MB/s between the module and the host. A flexible data packet system implemented over the PCIe interface provides both high data rates to the host that is readily expandable for custom applications.

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02/23/16

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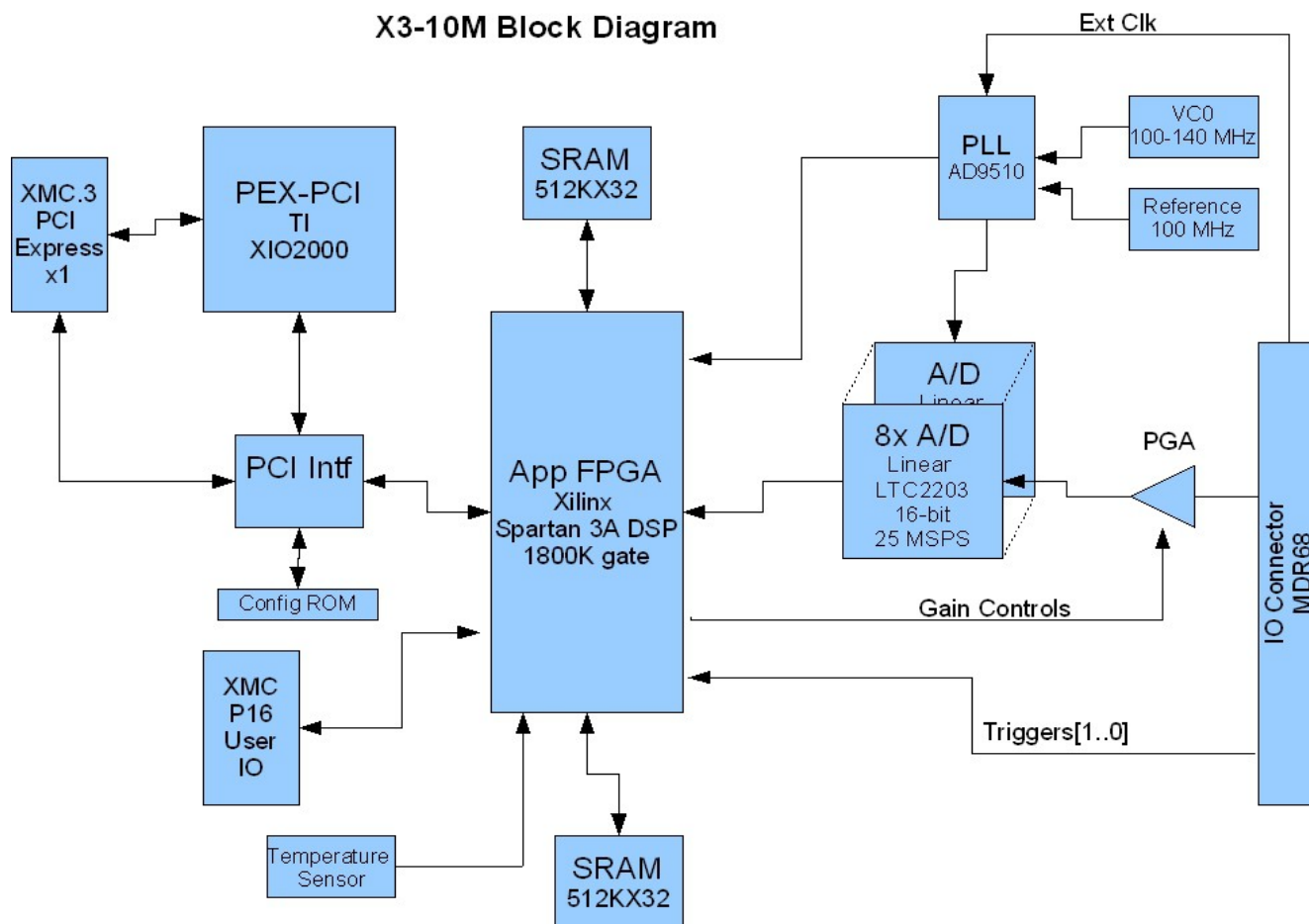
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ORDERING INFORMATION

See available board configurations and options online [here](#).

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X3-10M Block Diagram



X3-10M

Standard Features

Analog	
Inputs	8
Input Ranges	Programmable: +/-2V, +/-1V, +/-0.4V and +/-0.2V
Input Type	Differential, DC coupled
Input Impedance	>1M ohm
A/D Device	Linear Technology LTC2203
A/D Resolution	16-bit
A/D Sample Rate	4 MHz to 21.5 MHz ** Decimation feature in logic used for lower data rates ** 25 MHz possible w/custom firmware
Data Format	2's complement, 16-bit integer
Connector	MDR68
Calibration	Factory calibrated. Gain and offset errors are digitally corrected in the FPGA. Non-volatile EEPROM coefficient memory.

FPGA	
Size	1.8M gate equivalent (standard device)
Flip-Flops	33,280
DSP48A Elements	84
CLB	4160
Block RAMs	84 (1512K bits)
FPGA Device	Xilinx Spartan3A DSP XC3SD1800A-4FGG676C
Configuration	SelectMAP from PCIe interface JTAG during development
Clock Rate	83 MHz

Memory	
Size	4 MB total 2 devices @ 512Kx32 each
Type	Synchronous ZBT SRAM
SRAMs	Cypress CY7C1371D-133AXC
Uses	FPGA Buffer Memory FPGA computation memory

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Host Interface	
Type	PCI Express; single lane
Sustained Data Rate	180 MB/s
Protocol	Packet data
Connector	XMC P15
Interface Standard	PCIe 1.0a; VITA 42.3
Logic Update	In-system reconfiguration

Clocks and Triggering	
Clock Sources	PLL or External
PLL Output	4 MHz to 140 MHz
PLL Resolution	1530 Hz
PLL Jitter	<1 ps RMS
PLL Programming	Host programmed via PCIe
PLL Reference	Internal: 100 MHz clock External reference : J16 input
Triggering	External, software, acquire N frame
Decimation	1:1 to 1:4095 in FPGA
Channel Clocking	All channels are synchronous
Multi-card Synchronization	External triggering, clock, and PLL reference are supported.

Acquisition Monitoring	
Alerts	Trigger, Queue Overflow, Channel Over-range, Timestamp Rollover, Temperature Warning, Temperature Failure, PLL Unlocked
Alert Timestamping	15 ns resolution, 32-bit counter

P16 Digital IO	
Total Number of Bits	44
Balanced Pairs	22
Signal Standard	LVTTL Configurable as LVDS 2.5V
Drive	+/-12 mA (LVTTL)
Connector	XMC P16

Power Management	
Temperature Monitor	May be read by the host software
Alarms	Software programmable warning and failure levels
Over-temp Monitor	Disables analog IO power supplies
Power Control	Channel enables and power up enables
Heat Sinking	Conduction cooling supported. (subset of VITA20)

Physicals	
Form Factor	Single width IEEE 1386 Mezzanine Card
Size	75 x 150 mm
Weight	100g
Hazardous Materials	Lead-free and RoHS compliant

X3-10M

ABSOLUTE MAXIMUM RATINGS

Exposure to conditions exceeding these ratings may cause damage!

Parameter	Min	Max	Units	Conditions
Supply Voltage, 3.3V to GND	+3.0	+3.6	V	
Analog Input Voltage, Vin+ or Vin- to GND	-0.3	+6	V	
Operating Temperature	0	70	C	Non-condensing, forced air cooling required
Storage Temperature	-65	+150	C	
ESD Rating	-	1k	V	Human Body Model
Vibration	-	5	g	9-200 Hz, Class 3.3 per ETSI EN 300 019-1-3 V2.1.2 (2003-04)
Shock	-	40	g peak	Class 3.3 per ETSI EN 300 019-1-3 V2.1.2 (2003-04)

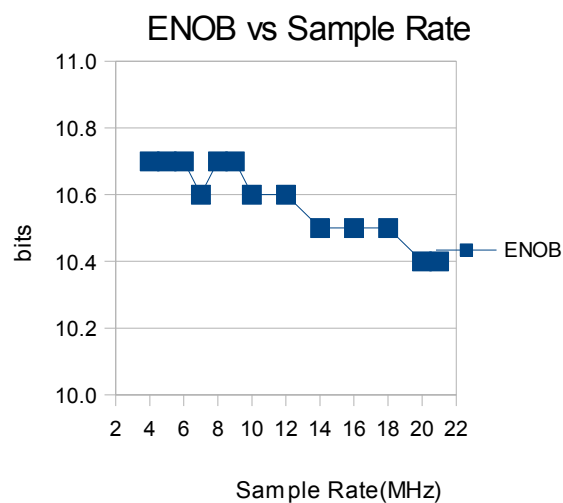
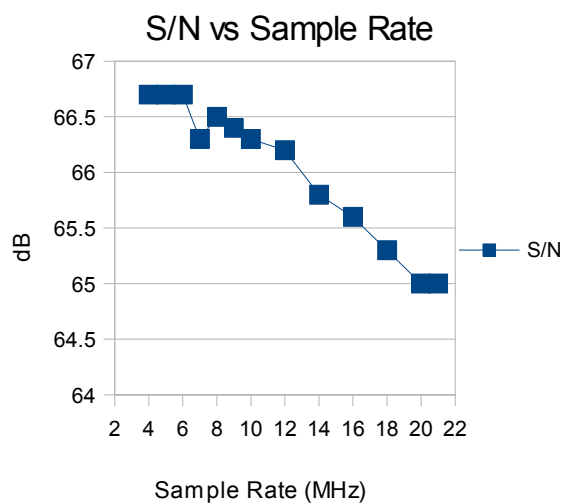
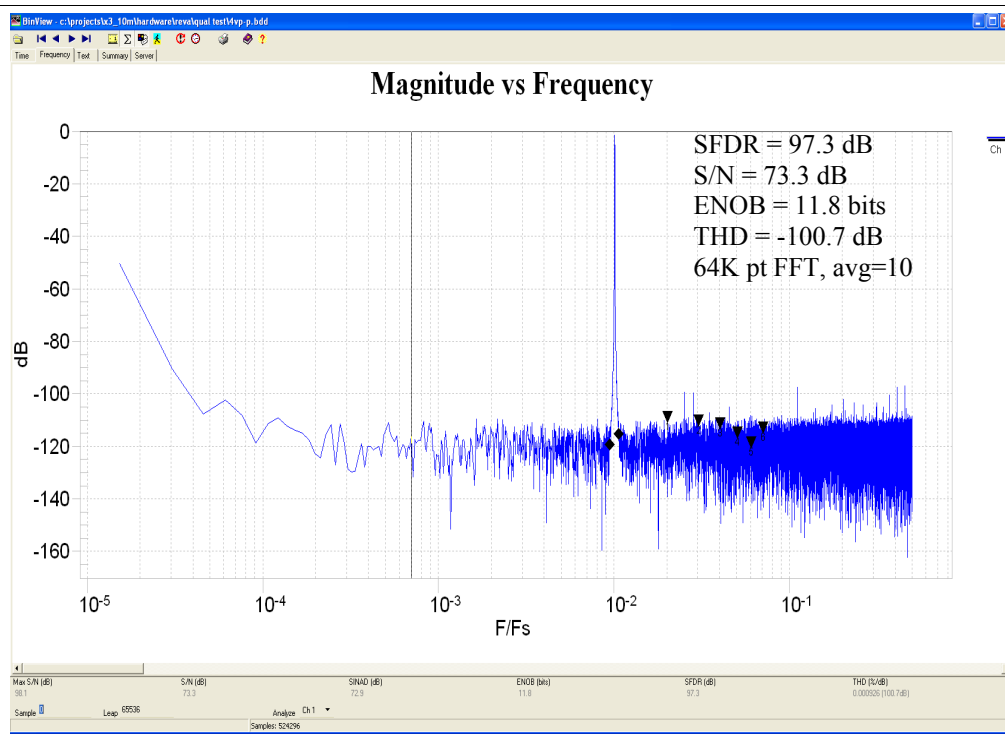
RECOMMENDED OPERATING CONDITIONS

Parameter	Min	Typ	Max	Units
Supply Voltage	+3.15	+3.3	+3.45	V
A/D Sampling Rate	4		25	MSPS
Operating Temperature	0		60	C

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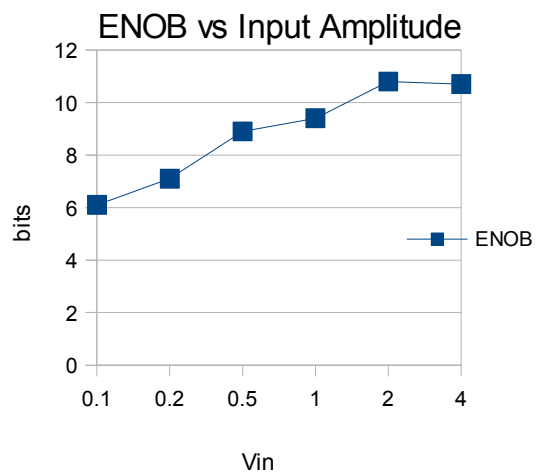
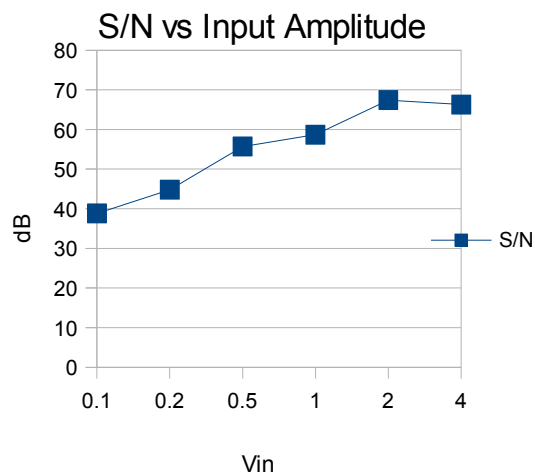
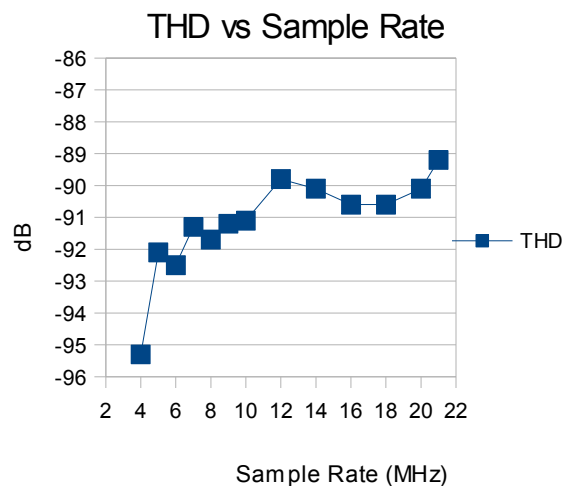
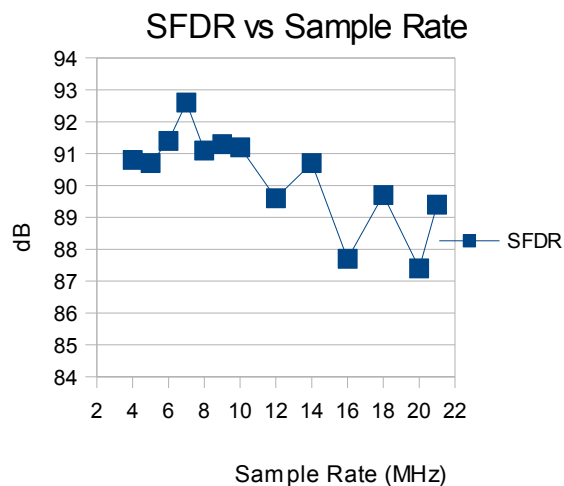
ELECTRICAL CHARACTERISTICS			
Over recommended operating free-air temperature range at 0°C to +60°C, unless otherwise noted.			
Parameter	Typ	Units	Notes
Analog Input			
Analog Input Bandwidth	6.5	MHz	-3dB @ G = 1 (see graphs)
SFDR	97.3	dB	10.1 kHz sine input, 4Vp-p differential, 64K point FFT avg of 10
S/N	73.3	dB	10.1 kHz sine input, 4Vp-p differential, 64K point FFT avg of 10
THD	100.7	dB	10.1 kHz sine input, 4Vp-p differential, 64K point FFT avg of 10
ENOB	11.8	dB	10.1 kHz sine input, 4Vp-p differential, 64K point FFT avg of 10
Intermodulation Distortion	-90	dB	9 kHz and 11 kHz sine, 2Vp-p each, differential
Common Mode Rejection	-100	dB	100 kHz, 4Vp-p input
Channel Crosstalk	-75	dB	100 kHz, 4Vp-p with MDR68 cable and screw terminal board
Noise	610	μV RMS	Grounded input.
Calibration			
Gain Error	<0.02	% of FS	Calibrated
Offset Error	<500	μV	Calibrated
Calibration Interval	1	year	
Power			
Supply Current	1.98	A	3.3V supply, all channels sampling at 10 MSPS, 27C ambient
Operating Temperature	48	C	No forced air in 27C ambient.

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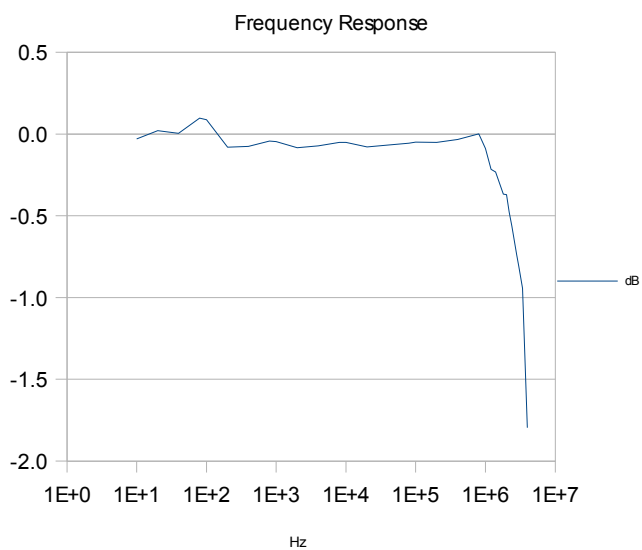
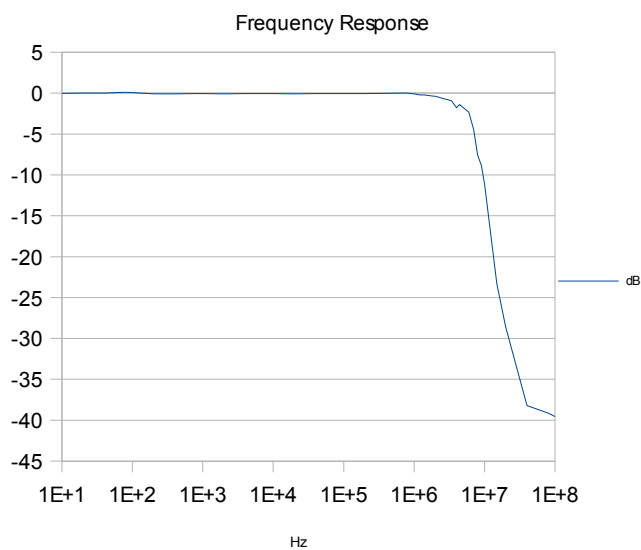
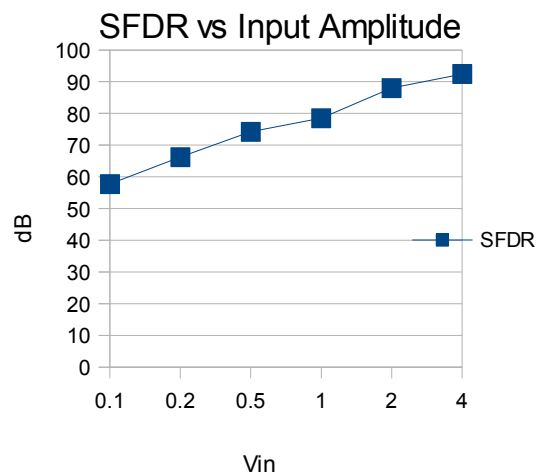
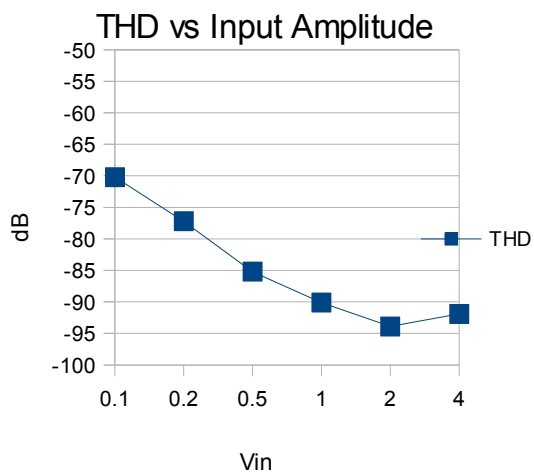


Note: All test results shown are 128K FFT no averaging.

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Architecture and Features

The analog front end of the X3-10M module has eight simultaneously sampling channels of 16-bit, 25 MSPS A/D input. All eight channels can be flowed continuously to the host PCIe at 10 MSPS. The A/D channels are high impedance differential inputs with programmable input ranges and an analog input bandwidth of 6 MHz at an analog gain of 1.

Controls for triggering and clocks allow precise control over the collection of data. Trigger modes include frames of programmable size, external and software. Multiple X3-10M cards can sample simultaneously using external trigger inputs with synchronized sample clocks. The sample clock can be external or generated from the on-card PLL. The PLL can either use the on-card 100 MHz reference, or can use an external reference. When an external reference is used, the sample clock is synchronous to the reference.

The X3 architecture has data buffering and a packet system to the host that provides an efficient and flexible host interface. The data buffer is a 1M sample SRAM that is used as a data queue. Data to the buffer is transferred to the host using the PCIe controller interface as data packets. The packet data system controls the flow of packets to the host, or other recipient, using a credit-based system managed in cooperation with the host software. The packets may be transmitted continuously for streams of data from the A/Ds, or as occasional packets for status, controls and analysis results. The data buffering and flow control system delivers high throughput with low latency and complete flexibility for data types and packet sizes to match the application requirements for all types of applications.

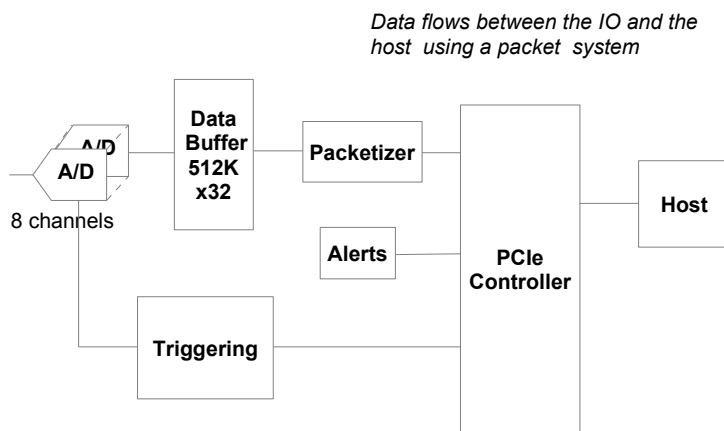
The data acquisition process can be monitored using the X3 alert mechanism. The alerts provide information on the timing of important events such as triggering, overranges and thermal overload. Packets containing data about the alert including an absolute system timestamp of the alert, and other information such as current temperature. This provides a precise overview of the card data acquisition process by recording the occurrence of these real-time events making the X3 modules easier to integrate into larger systems.

Software Tools

Software for data logging and analysis is provided with every X3 module. Data can be logged to system memory at full rate or to disk at rates supported by the drive and controller. Triggering, sample rate controls, and data logging features allow you to use X3 modules in your application without ever writing code. Innovative software applications include *Binview* which provides data viewing, analysis and export data to MATLAB for large data files, as well as support applications for logic loading, firmware updates and system configuration.

Software development tools for the X3 modules provide comprehensive support including device drivers, data buffering, card controls, and utilities that allow developers to be productive from the start. At the most fundamental level, the software tools deliver data buffers to your application without the burden of low-level real-time control of the cards. Software classes provide C++ developers a powerful, high-level interface to the card that makes real-time, high speed data acquisition easier to integrate into applications.

Support for MS Visual C++ is provided. Supported OS include Windows and Linux. For more information, the software



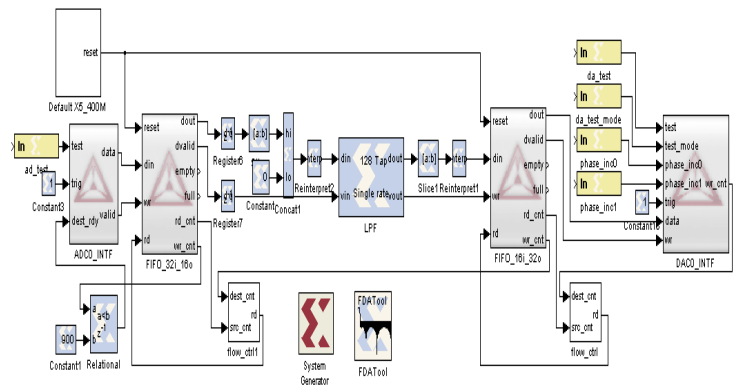
X3-10M Architecture

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tools and on-line help may be downloaded.

Logic Tools

High speed DSP, analysis, customized triggering and other unique features may be added to the X3 modules by modifying the logic. The FrameWork Logic tools support RTL and MATLAB developments. The standard logic provides a hardware interface layer that allows designers to concentrate on the application-specific portions of the design. Designer can build upon the Innovative components for packet handling, hardware interfaces and system functions, the Xilinx IP core library, and third party IP. RTL source for the FrameWork Logic is provided for customization. Each design is provided as a Xilinx ISE project, with a ModelSim testbench illustrating logic functionality.



The MATLAB Board Support Package (BSP) supports logic development using Simulink and Xilinx System Generator. These tools provide a graphical design environment that integrates the logic into MATLAB Simulink for complete hardware-in-the-loop testing and development. The MATLAB tools are an extremely powerful design methodology that can be used to generate, analyze and display the signals in the logic real-time in the system. Once the development is complete, the logic can be embedded in the FrameWork logic using the Xilinx ISE tools.

The FrameWork Logic User sales brochure and User Guide more fully detail the development tools.

Applications Information

Maximum A/D Sample Rates

For the standard FrameWork logic, the A/D sample rates are limited by the destination of the data as shown in the following table. Custom logic implementations can achieve full 25 MSPS rates from all channels into the logic.

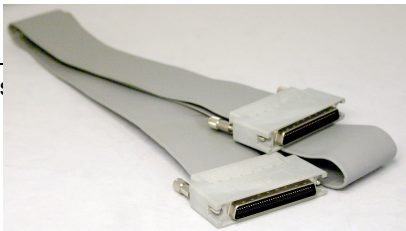
A/D Sample Destination	Maximum Sample Rate
FPGA logic	21.5 MSPS per channel. (25 MSPS possible w/custom firmware).
On-module data buffer	8 channels at 10 MSPS each, 2 channels at 21.5 MSPS each
Host PCIe system memory	8 channels at 10 MSPS, 4 channels at 21.5 MSPS, 2 channels at 21.5 MSPS

Maximum Data Rates

The maximum data rates supported by the module are limited by the PCI Express transfer rate when the total data rate exceeds 160 MB/s. The PCI Express transfer rate may vary according to the host computer, operating system, and other system activity that may compete for bandwidth. The X3 modules support 250MB/s full duplex during bursts, but actual sustained throughput is 160 MB/s in typical desktop PCs.

It is important to qualify systems for performance when data rates approach 160 MB/s.

This rate limitation does not apply to data generated in the FPGA.



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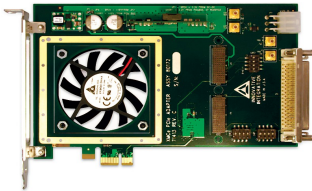
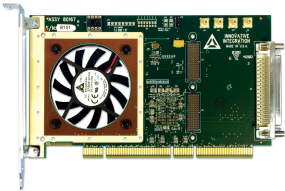

Cables

X3 modules use a shielded, jacketed 68-wire cable assembly for the front panel IO. The pleated copper foil shield cable is “near coax” in its performance. This cable, plus the use of differential signals and use of ground signals as shields, produce the best results. A screw terminal assembly is available. See available cable options online [here](#).

XMC Adapter Cards

XMC modules can be used in standard desktop system, compact PCI/PXI using an adapter card. Adapters for cabled PCI Express (CPEX) and VPX are also available. All adapter cards are software transparent.

The X3 modules use the auxiliary P16 connector for digital IO and additional clock inputs. A total of 44 bits of digital IO, directly connected to the application FPGA, are routed to the rear edge MDR connector as 22 balanced differential pairs supporting LVDS or lower speed single-ended LVC MOS signals. The X3 modules also have a sample clock input and PLL reference input to J16. The cPCI/PXI adapter uses these to connect to system clocks, while the PCIe desktop adapter provides SMB input connectors for system clock inputs. See available carrier options online [here](#).

<p>PCIe-XMC Adapter (80172) x1 PCIe to XMC SMB Clock and trigger inputs</p> 	<p>PCI-XMC Adapter (80167) 64-bit, 133 MHz PCI-X host x4 PCIe to XMC</p> 	<p>Compact PCI-XMC Adapter (80207) 64-bit, 133 MHz PCI-X host x4 PCIe to XMC PXI triggers and clock support</p> 
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X3-10M

Applications that need remote or portable IO can use either the eInstrument PC or eInstrument Node with X3 modules. See available intelligent carrier options online [here](#).

eInstrument PC with Dual PCI Express XMC Modules (90201)

Windows/Linux embedded PC
8x USB, GbE, cable PCIe, VGA
High speed x8 interconnect between modules
GPS disciplined, programmable sample clocks and triggers to XMCs
Up to 400MB/s data logging using SSD
12V operation



eInstrument PC with Dual PCI Express XMC Modules (90271)

Windows/Linux embedded PC
6x USB, GbE, 8x cable PCIe, DisplayPort
High speed x4 PCIe + Aurora interconnect between modules
GPS disciplined, programmable sample clocks and triggers to XMCs
Up to 500MB/s data logging using SSD



eInstrument DAQ Node – Remote IO using cabled PCI Express (90181)

PCI Express system expansion
Up to 7 meter cable
electrically isolated from host computer
software transparent



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