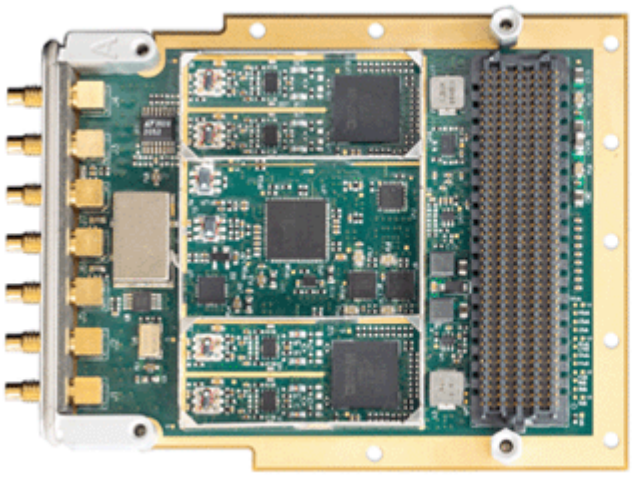
# Passive Radar Receiver Using FMC-1000

In 2015 Entegra Solutions were contacted by Thales Air Traffic Management looking for the highest dynamic range, wide bandwidth data acquisition card available. Their objective was to build a passive radar using beamforming techniques to receive reflections of DVB-T Tv signals from aircraft to replace traditional airfield radars. Their requirement was simple, the highest SFDR possible, ideally direct sampling of the UHF signal, followed by digital receivers with FPGA for beamforming.

Entegra Solutions Ltd has been the UK value added reseller of solutions by Innovative Integration Inc since 1999, with a history of supplying many data acquisition solutions complete with software, logic and support. After several technical discussions, Entegra were able to propose a multistage project with steps of integrating the latest hardware from Innovative to provide a roadmap to the best long term solution. The first stage is documented below.

The first stage was to prove that it was possible to acquire and extract real reflections of DVB-T signals from aircraft using a dual aerial receiver. The newest available Adc module suitable for the project was the FMC-1000.



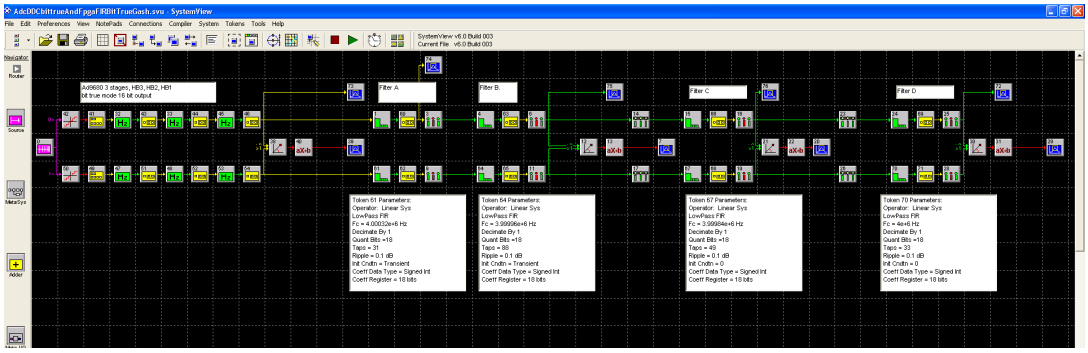
The FMC-1000 has the Analog Devices AD9680-1000 (1) at its heart, which is a dual 1000MSPS 14-bit Adc with a SFDR of 82dBFS in the second Nyquist zone. This enabled the front end to do direct sampling, ie no form of frequency shifting was required of the analogue signal before digitisation. Direct sampling would make the coherent beamforming easier and more accurate. It also saves the cost of RF analogue downconversion. The AD9680 also has four channels of coarse oscillator and digital down conversion built in. For signal generation the FMC-1000 has the DAC38J82, dual 1230MSPS 16-bit Dac and a LMK04828 PLL for ultra low noise clock generation.

FMC modules need a FMC host. At the time (2) the ePC-K7 was the only FMC host available from Innovative. It would have been possible to use third party FMC hosts, however it is not a trivial engineering task to support complex FMC modules such as the FMC-1000 on third party hosts, the JESD204B serial lanes that stream data to and from the Adcs and Dacs need significant attention to detail alone to achieve reliable operation. The ePC-K7 has a FMC HPC site with a direct connection to a Xilinx Kintex-7 FPGA, hosted by an Intel i7 CPU with memory, graphics, SATA, USB, dual ethernet etc. The ePC-K7 is a conduction cooled standalone unit, shown below.

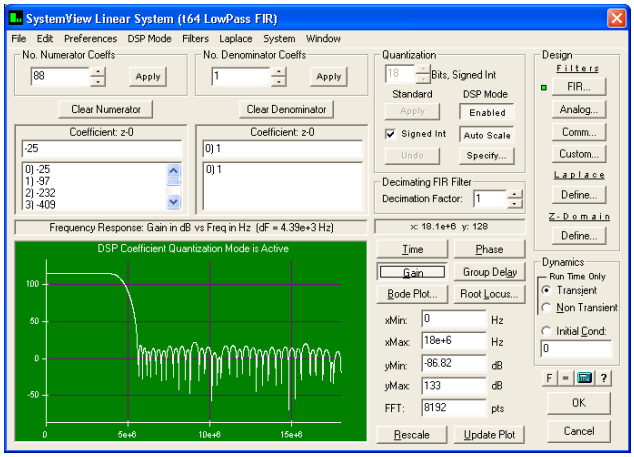

Thales already had algorithms written to demodulate DVB-T signals far enough to extract the start of each frame and therefore the time of arrival of a frame. This could be used to extract both the direct signal from the Tv broadcast aerial and any reflected (delayed) signals. By having multiple receivers at different known locations, time of arrival pulses could be triangulated to determine the location of reflections. The algorithms required an input signal of the DVB-T baseband complex signal which is 64/7MSPS.

The receiver had to cover the DVB-T UHF band used in the UK, which covers 470-850MHz. A sample rate of 864MSPS was selected which required an overall digital receiver decimation of 94.5 to get to 64/7MSPS. Innovative Integration supply digital receiver IP for the ePC-K7, but this does not include interpolation therefore some new digital receiver IP had to be developed for the FPGA.

The first step of the digital receiver design process was to use SystemView, a DSP algorithm simulator that Entegra used to supply across Europe before the product was assimilated into Agilent Technologies. The filter stages, decimation and interpolation was simulated both in floating point mode and bit true integer mode to evaluate design choices so that the minimum of FPGA resources were used. At this stage it was not known how many other resources would be needed for beamforming and possibly the early stages of demodulation.

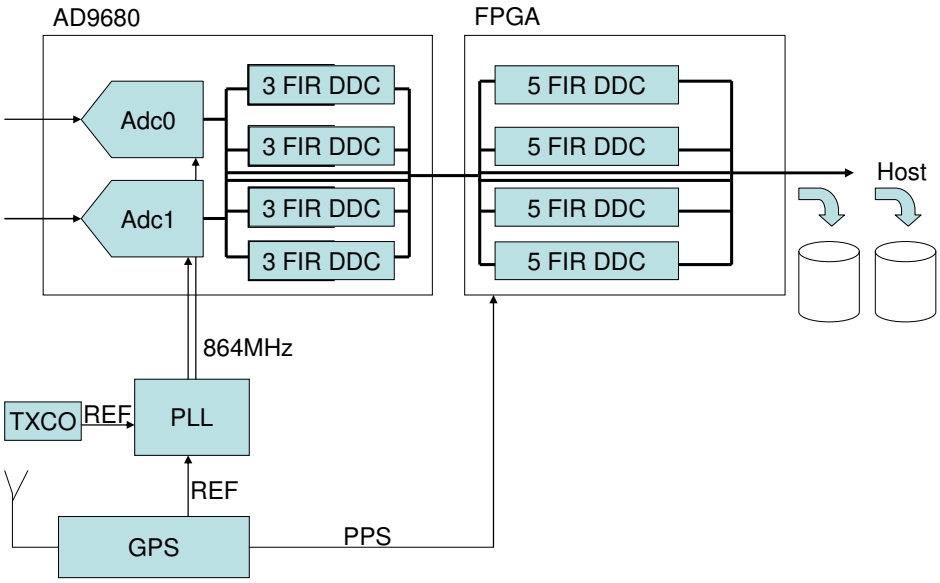


*Block based simulation of digital receivers in the Adc and FPGA*




*Filter design with bit true simulation*

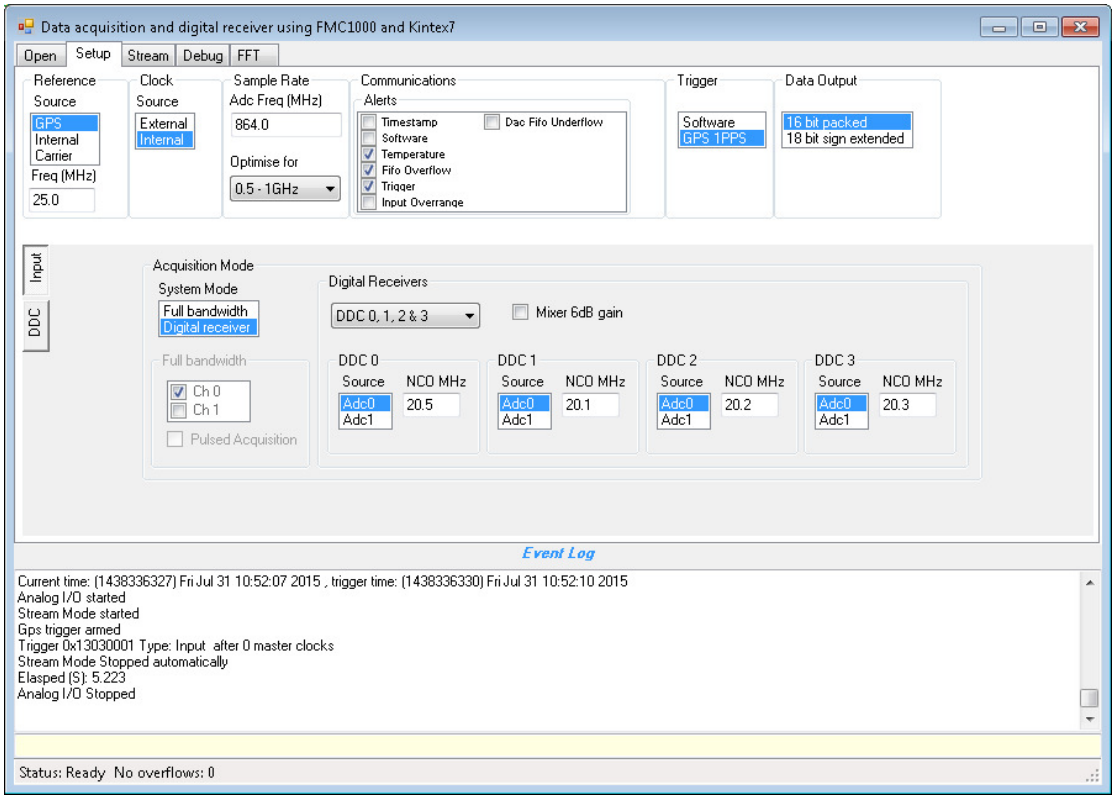
The second stage was to implement the five stages of filtering into VHDL code. The first four stages were for decimation, interpolation and band reduction. The fifth stage was simply for compensating for the combined passbands having some ripple so that the overall passband was flat to +/-0.1dB. Vivado is used for development with Xilinx Kintex-7 FPGA's so this was used for logic development. The Vivado IDE has the ability to display datasets as time waveforms, so this was useful to check that filters were behaving as expected. The IP Catalog has support for FIR filters and digital oscillators. Once the receivers were developed in isolation, the project was ready for the third stage.



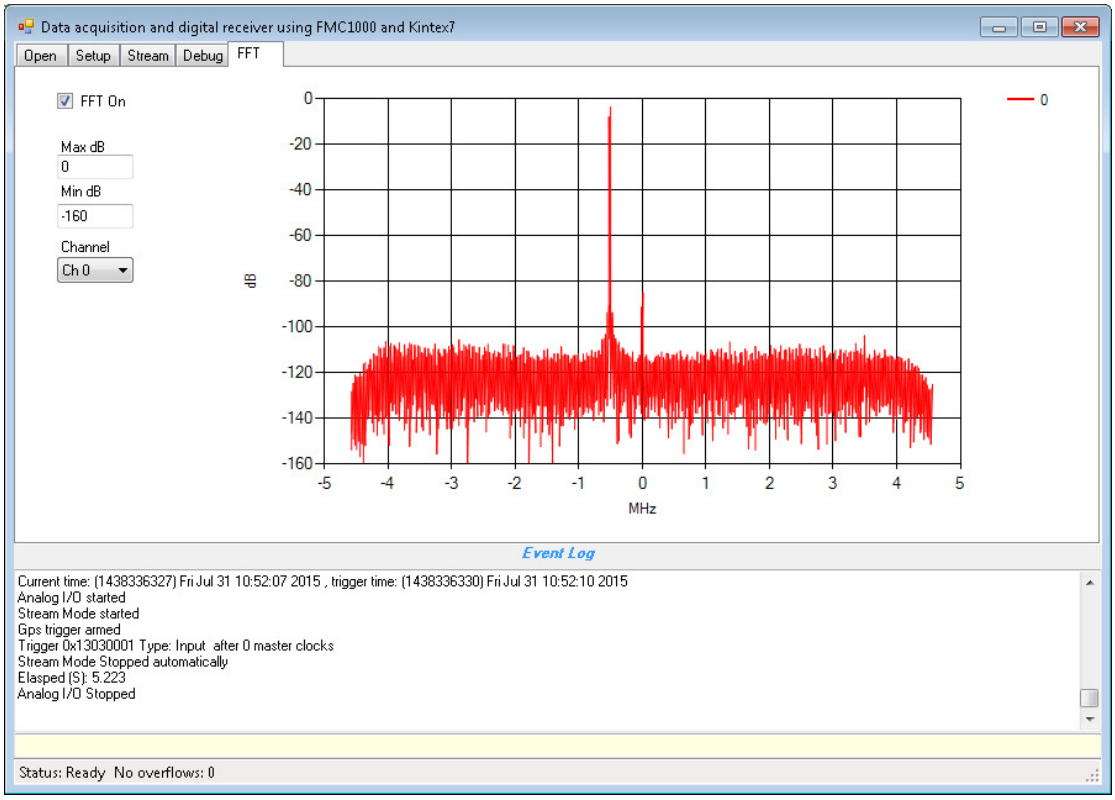

*Overall signal processing system diagram*

The third stage was to add the receivers to the IP already shipped with the ePC-K7 & FMC-1000. Innovative Integration call this the Framework Logic because it provides all of the necessary logic to make the system work as a data acquisition solution. This includes controlling Adc's, Dac's, PLL's, loading and maintaining configuration from EEPROM, using attached DDR3 memory as FIFO's, stream data from Adc's to the host and data from the host to Dac's, adding timing and packet information using VITA 49, and the PCIe x8 lane gen 2 port. The product provides a framework for designers to be able to insert their signal processing at the appropriate stage. Innovative's Framework Logic uses the Wishbone interface which makes it very easy for developers to add control and status registers into the large FPGA with very little effort.

The fourth stage was to write the host software that would run on the Intel i7 CPU running under Windows to control the acquisition and storage of data. Innovative provide several example programs per FMC module, so again, we had something which worked already and just needed modification to suit the application. Their Malibu toolset provided all of the C++ libraries and utilities that were required for development. Controls were added to manage the new receivers in the logic and a real time FFT graph was provided which could either display the spectrum of a receiver channel or the entire bandwidth of the Adc with no downsampling. An external dual disc RAID box was provided to increase storage capacity and provide an easy method of removing discs.




*Graphical User Interface for control and monitoring*




*Real time spectrum of one digital receiver channel output*

The ePC-K7 is available with optional GPS receiver. This was used to get the 1PPS so that sampling could be set to start at a predetermined UTC time. This meant that recorded data could be post processed offline through demodulation algorithms and

compared against known aircraft movements at the time of recording. The data is formatted with VITA 49 timestamps for easy identification. The 10MHz reference output can also be used for generating the sample clock, although step adjustments made to some GPS disciplined can make that unfavourable for receivers.


*Front of ePC-K7 showing analogue inputs and GPS connections*

Bart Barnes, Senior Surveillance Engineer said ‘For advanced radar systems Thales is looking for a partner that can work at the cutting edge of technology yet deliver COTS based solutions. Entegra have delivered this on time with expertise and support to back this up.’

John Owen, Technical Director, Entegra Solutions Ltd. John.owen@entegra.co.uk

Notes

1. The FMC-1000 is also available with the AD9680-1250 1250MSPS 14 bit part
2. Innovative Integration Inc have designed other FMC hosts including COPious-PCIe, COPious-PXIe, Cardsharp, mini-K7.