X3-A4D4

v1.2

PCI Express XMC Module with Four 4 MSPS A/Ds, Four 50 MSPS DACs and 1.8M Spartan3A DSP FPGA

FEATURES

- Four 4 MSPS, 16-bit A/D channels
- 12.3 bit ENOB, 92 dB SFDR A/Ds
- Four 50 MSPS, 16-bit DAC channels
- Differential instrumentation inputs with +/-10V, +/-5V, +/-2.5V, +/-1.25V input ranges
- +/-10V output range
- Low Latency I/O for servo controls
- Xilinx Spartan3A DSP 1.8M or 3.4M FPGA
- 4MB SRAM
- 16 Digital IO's on JP1
- Programmable or external sample clock
- Synchronized system sampling using common reference clock and triggers
- Framed, software or external triggering
- Log acquisition timing and events
- 44 bits digital IO on P16
- Power Management features
- PCI Express XMC Module (75x150 mm)
- Use in any PCI Express desktop, compact PCI/PXI, or cabled PCI Express application

APPLICATIONS

- Servo Controls
- Stimulus-response measurements
- Arbitrary Waveform Generation

SOFTWARE

- Data Acquisition, Logging and Analysis applications provided
- Windows/Linux Drivers
- C++ Host Tools
- VHDL/MATLAB Logic Tools

DESCRIPTION

The X3-A4D4 is an XMC IO module featuring four 16-bit, 4 MSPS A/D channels and four 16-bit, 50 MSPS DAC channels with FPGA computing core designed for servo controls, arbitrary waveform generation and stimulus-response applications. Low latency SAR A/D and no-pipeline DACs support real-time servo control applications.

Flexible trigger methods include N-point frames, software triggering and external triggering. The sample clock is either an external clock or on-board programmable PLL clock source. The PLL can lock to an external reference.

Data acquisition control, signal processing, buffering, and system functions are implemented in a Xilinx Spartan3A DSP 1.8M FPGA device. Two 512Kx32 memories are used for data buffering and FPGA computing memory.

The logic can be fully customized using VHDL and MATLAB using the FrameWork Logic toolset. The MATLAB BSP supports real-time hardware-in-the-loop development using the graphical, block diagram Simulink environment with Xilinx System Generator.

The PCI Express interface supports continuous data rates up to 180 MB/s between the module and the host. A flexible data packet system to the PCIe interface provides fast data transfers to the host that readily adapts to custom applications.

05/08/13

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This electronics assembly can be damaged by ESD. Innovative Integration recommends that all electronic assemblies and components circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

Product	Part Number	Description
X3-A4D4	80177-0	XMC module with four 4MSPS A/D , four 50 MSPS DACs, 1.8M gate FPGA, 4MB SRAM
X3-A4D4	80177-1	PCI EXPRESS-PCIe XMC MODULE w/3.4 MG Spartan3A FPGA
Logic		
X3-A4D4 FrameWork Logic	55021	X3-A4D4 FrameWork Logic board support package for RTL and MATLAB. Includes technical support for one year.
Cables		
MDR68 cable	65057	IO cable with MDR68 plug on each end, 3 feet length (0.92m)
MDR68 breakout	80116-0	Breakout module with MDR68 Connector and screw terminal connection
PCIe cable	67057	Single Lane PCI Express Cable - 5m
PCIe cable	67058	Single Lane PCI Express Cable - 3m
PCIe cable	67059	Single Lane PCI Express Cable - 1m
Breakout cable	67079	X3-A4D4 Breakout cable, cable assembly provides coax cables with BNC termination
Cable x4PCI express	67098	Cable x4PCI express, 1 meter
Breakout	80112-1	MDR68-female to screw terminal block
MDR cable	80116-1	68-pin and screw terminal block
Adapters		
XMC-PCIe x1 Adapter	80172-0	PCI Express Carrier card for XMC PCI Express modules, x1 lanes
PCIe X1 Cable Adapter	80181-0	Desktop PCI Express X1 Cable Adapter
PCIe X1 Cable Adapter	80186-0	Laptop PCI Express X1 Cable Adapter
XMC to CompactPCI Adapter	80207-0	CompactPCI to XMCe Adapter Board
cPCI-XMCe Adapter	80207-1-L4	cPCI-XMCe Adapter 3U Conduction Cooled
CPEX4	80246-0	X4 PCI Express Cable adapter card

XMC Adapter for 3U OpenVPX	80260-3	VPX-XMC 3U ADAPTER, conduction cooled, without REDI covers for X3 modules
XMC Adapter for 3U OpenVPX	80260-3RC	VPX-XMC 3U ADAPTER, conduction cooled, with REDI covers for X3 modules
XMC Adapter for 3U OpenVPX	80260-3RCA	VPX-XMC 3U ADAPTER, conduction cooled, with REDI covers for X3 modules & assembly
XMC-PCI Adapter	80167	PCI Carrier card for XMC PCI Express modules, 64-bit PCI-X
XMC-cPCI Adapter	80207	3U Compact PCI/PXI Carrier card for XMC PCI Express modules, 64-bit PCI-X
XMC-Cabled PCIe Adapter	90181	Cabled PCI Express Carrier card for XMC PCI Express modules, single-lane.
eInstrument-DAQ Node	90181-0	XMC module carrier with 2.5 Gbps cabled PCI Express link to Host Computer housed in a rugged aluminum enclosure.
CPEX4 Hub	90241-0	Cabled PCI Express 4-port Hub including chassis
XMC Modules		
X3-Timing	80234-0	MDR cable 68-pin and screw terminal block
X3-Timing	80234-2	PCI Express XMC Module, 500 ppb crystal, with GPS
Embedded PC Host		
eInstrument PC	90199	Embedded PC XMC host with support for two XMC modules for standalone applications.
IP Blocks		
IP-XLFFT	58011-0	Core for 64K to 1M points FFT for 1-D, 2-D signal Netlist undle with hardware
IP-XLFFT	58011-1	Core for 64K to 1M points FFT for 1-D, 2-D signal Netlist
IP-WINDOWING	58012-0	Run-time configurable Hann, Blackman, and Boxcar data windowing functions Netlist bundle with hardware
IP-WINDOWING	58012-1	Run-time configurable Hann, Blackman, and Boxcar data windowing functions Netlist

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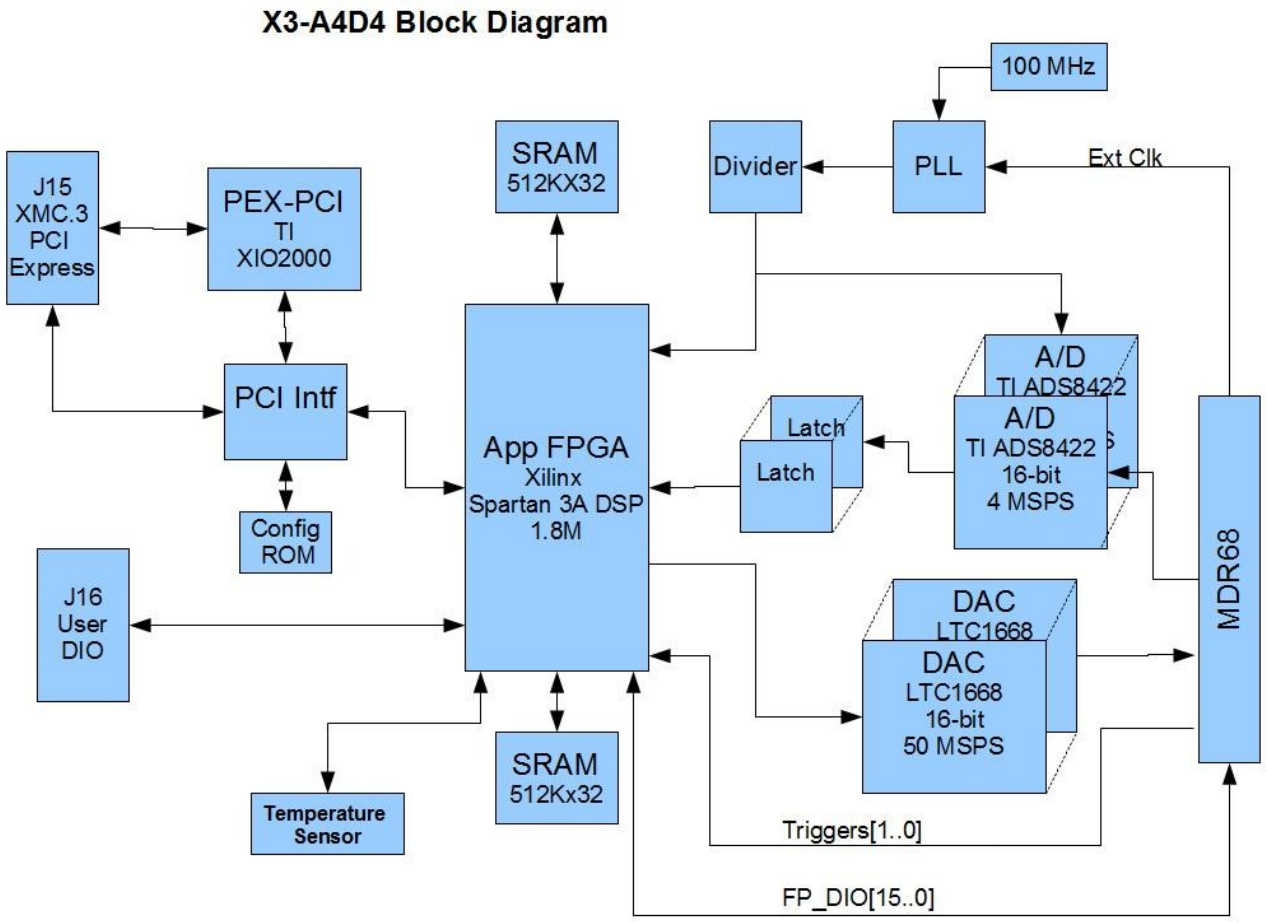
X3-A4D4 Block Diagram
100 MHz
PLL
Divider
Ext Clk
SRAM
512KX32
J15
XMC.3
PCI
Express
PEX-PCI
TI
XIO2000
PCI Intf
Config
ROM
App FPGA
Xilinx
Spartan 3A DSP
1.8M
Latch
Latch
A/D
TI ADS8422
16-bit
4 MSPS
A/D
TI ADS8422
J16
User
DIO
DAC
LTC1668
DAC
LTC1668
16-bit
50 MSPS
MDR68
SRAM
512Kx32
Temperature
Sensor
Triggers[1..0]
FP_DIO[15..0]

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Standard Features

Analog	
Inputs	4
Input Ranges	Programmable: +/-10V, +/-5V, +/-2.5V, +/- 1.25V
Input Type	Differential, DC Coupled
Input Impedance	>1M ohm
A/D Device	Texas Instruments ADS8422
A/D Resolution	16-bit
A/D Sample Rate	4 MSPS
Outputs	4
Output Range	+/-10V
Output Type	Single ended, DC coupled
Output Impedance	<1 ohm
DAC Device	Linear Technology LTC1668
DAC Resolution	16-bit
DAC Sample Rate	DC to 50 MHz** ** Data rate from PCIe limited to ~10MHz per channel when all 4 channels are in use
Data Format	2's complement, 16-bit integer
Connector	MDR68
Calibration	Factory calibrated. Gain and offset errors are digitally corrected in the FPGA. Non-volatile EEPROM coefficient memory.

FPGA	
Size	1.8M gate equivalent
Flip-Flops	33,280
Multipliers	84
CLB	4160
Block RAMs	84 (1512K bits)
FPGA Device	Xilinx Spartan3A DSP XC3SD1800A-4FGG676C
Configuration	SelectMAP from PCIe interface JTAG during development
Clock Rate	107 MHz system clock

Memory	
Size	4 MB total 2 devices @ 512Kx32 each
Type	Synchronous ZBT SRAM
SRAMs	Cypress CY7C1371D-133AXC
Uses	FPGA Buffer Memory FPGA computation memory
Clock Rate	107 MHz

Reliability	
MTBF	106,301

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Host Interface	
Type	PCI Express; single lane
Sustained Data Rate	180 MB/s
Protocol	Packet data
Connector	XMC P15
Interface Standard	PCIe 1.0a; VITA 42.3
Logic Update	In-system reconfiguration

Clocks and Triggering	
Clock Sources	PLL or External
PLL sample rates	10 kHz 140 MHz
PLL Resolution	48 Hz
PLL Jitter	<1 ps RMS
PLL Programming	Host programmed via PCIe
PLL Reference	Internal: 100 MHz clock External reference : J16 input
Triggering	External, software, acquire N frame
Decimation	1:1 to 1:4095 in FPGA
Channel Clocking	All channels are synchronous
Multi-card Synchronization	External triggering, clock, and PLL reference are supported.

Acquisition Monitoring	
Alerts	Trigger, Queue Overflow, Channel Over-range, Timestamp Rollover, Temperature Warning, Temperature Failure, PLL Unlocked
Alert Timestamping	15 ns resolution, 32-bit counter

P16 Digital IO	
Total Number of Bits	44
Balanced Pairs	24
Signal Standard	LVTTL Configurable as LVDS 2.5V
Drive	+/-12 mA (LVTTL)
Connector	XMC P16

Power Management	
Temperature Monitor	May be read by the host software
Alarms	Software programmable warning and failure levels
Over-temp Monitor	Disables analog IO power supplies
Power Control	Channel enables and power up enables
Heat Sinking	Conduction cooling supported. (subset of VITA20)

Physicals	
Form Factor	Single width IEEE 1386 Mezzanine Card
Size	75 x 150 mm
Weight	100g
Hazardous Materials	Lead-free and RoHS compliant

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ABSOLUTE MAXIMUM RATINGS

Exposure to conditions exceeding these ratings may cause damage!

Parameter	Min	Max	Units	Conditions
Supply Voltage, 3.3V to GND	+3.0	+3.6	V	
Analog Input Voltage, Vin+ or Vin- to GND	-12	+12	V	
Operating Temperature	0	70	C	Non-condensing
Storage Temperature	-65	+150	C	
ESD Rating	-	1k	V	Human Body Model
Vibration	-	5	g	9-200 Hz, Class 3.3 per ETSI EN 300 019-1-3 V2.1.2 (2003-04)
Shock	-	40	g peak	Class 3.3 per ETSI EN 300 019-1-3 V2.1.2 (2003-04)

RECOMMENDED OPERATING CONDITIONS

Parameter	Min	Typ	Max	Units
Supply Voltage	+3.15	+3.3	+3.45	V
A/D Sampling Rate	-		4000	MSPS
DAC Sampling Rate	-		50000	MSP
Operating Temperature	0		70	C

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ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range at 0°C to +70°C, unless otherwise noted.

Parameter	Typ	Units	Notes
Analog Input			
Analog Input Bandwidth	600	kHz	-3dB point.
A/D SFDR	92	dB	1.01kHz sine input, 10Vp-p, Fs = 4MSPS
A/D S/N	76	dB	1.01kHz sine input, 10Vp-p, Fs = 4MSPS
A/D THD	-114	dB	1.01kHz sine input, 10Vp-p, Fs = 4MSPS
A/D ENOB	12.3	dB	1.01kHz sine input, 10Vp-p, Fs = 4MSPS
A/D Latency	500	ns	Measured from analog input to after error correction in the FPGA
A/D Channel Crosstalk	<-100	dB	1.01 kHz, 19Vp-p input, cable included, all channels
A/D Noise	1221	µV p-p	Input Grounded, sample rate = 3.9 MSPS, 250k samples
A/D Noise Floor	<-108	dB	Input Grounded, sample rate = 3.9MSPS, 64K sample FFT, non-averaged
Analog Output			
Analog Output Bandwidth	2.5	MHz	<0.4 dB variation across range
DAC SFDR	84	dB	1.224 kHz sine input, 10Vp-p, 10 MSPS
DAC S/N	97	dB	1.224 kHz sine input, 10Vp-p, 10 MSPS
DAC THD	-78	dB	1.224 kHz sine input, 10Vp-p, 10 MSPS
DAC ENOB	12.6	dB	1.224 kHz sine input, 10Vp-p, 10 MSPS
DAC Latency	400	ns	Measured from FPGA sample to analog output after settling
DAC Channel Crosstalk	<-100	dB	1 kHz, 19Vp-p sine on active channel input, cable included, all channels, at noise floor
DAC Noise	1750	µV RMS	Output commanded to 0V, update rate = 1MSPS
DAC Noise Floor	<-100	dB	Output commanded to 0V, update rate = 1MSPS, 0 to 100kHz span. At limit of measurement.
Calibration			
Offset Calibration Accuracy	<0.01	%FS	Factory calibration in each analog range.
Gain Calibration Error	<0.02	% of FS	Factory calibration in each analog range.
Calibration Interval	1	year	
Power			
Power Consumption	8	W	Typical for 24C ambient and 5 CFM air flow.

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Analog Input Performance Data

Analog Output Spectral Purity

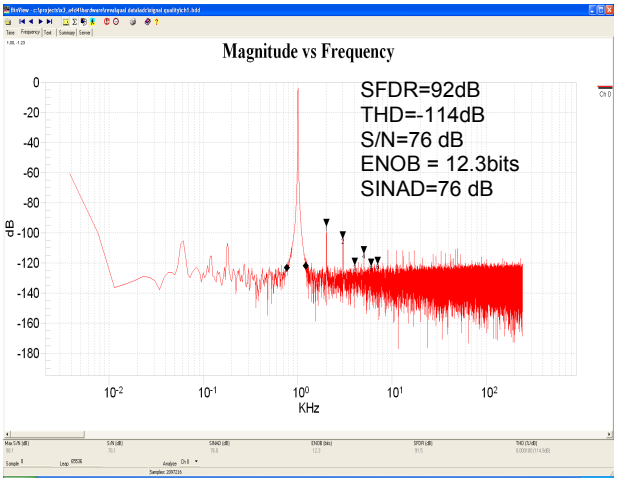


Figure 1. Signal quality measurement (1.01 kHz input, 10Vp-p, sample rate = 1 MSPS)

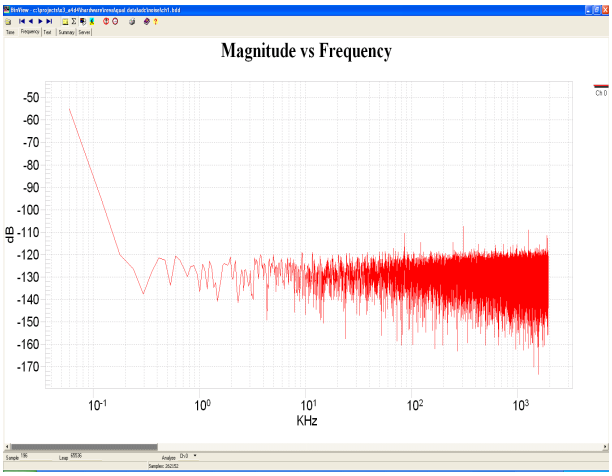
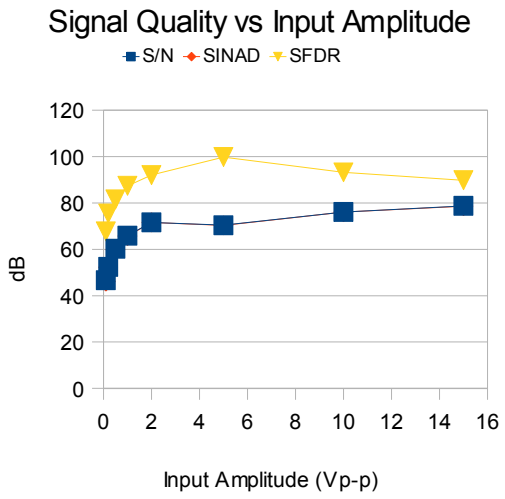
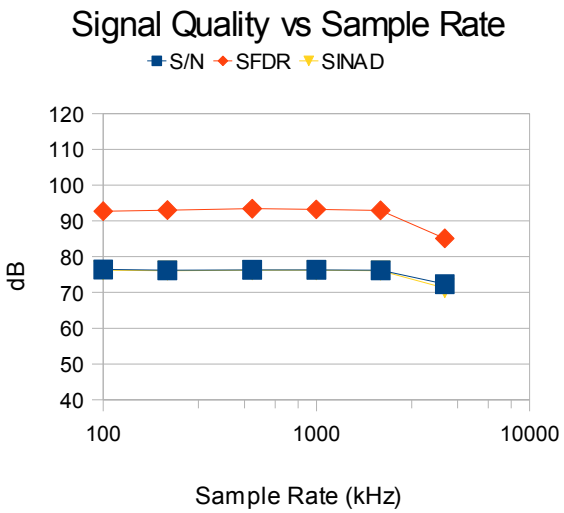


Figure 2. Noise floor (grounded input, Fs= 3.888 MSPS)





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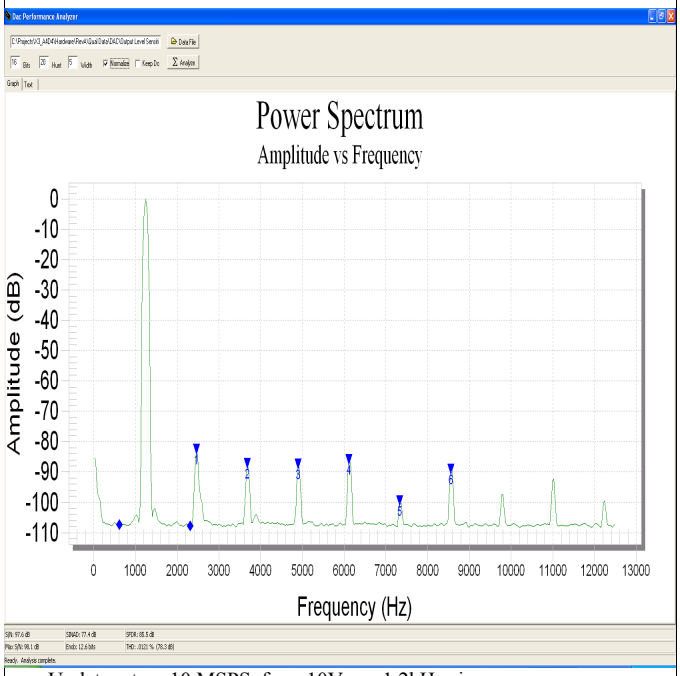
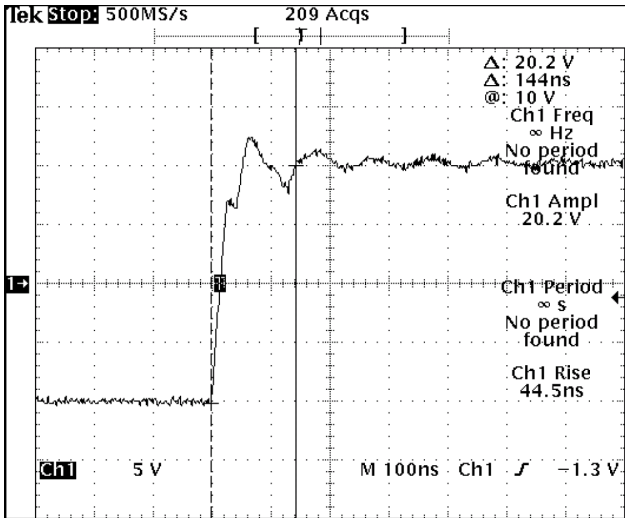
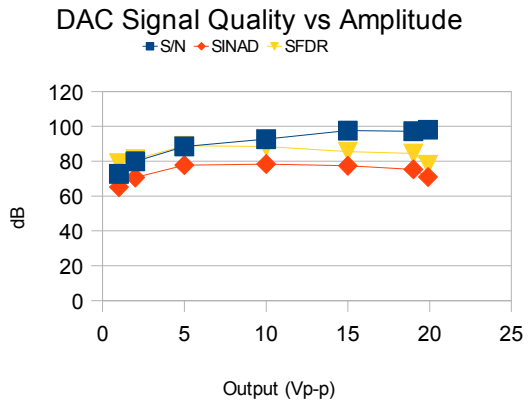
Analog Output Performance Data

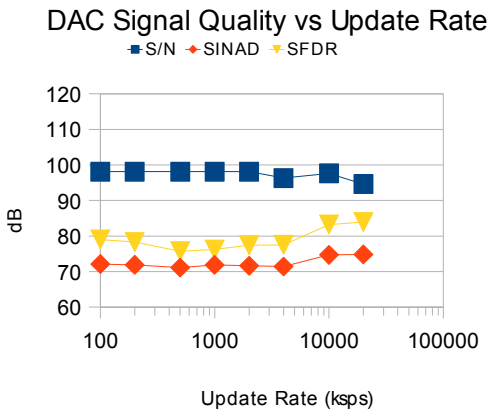


Update rate = 10 MSPS, for a 10Vp-p, 1.2kHz sine

Output Settling for 20V Step





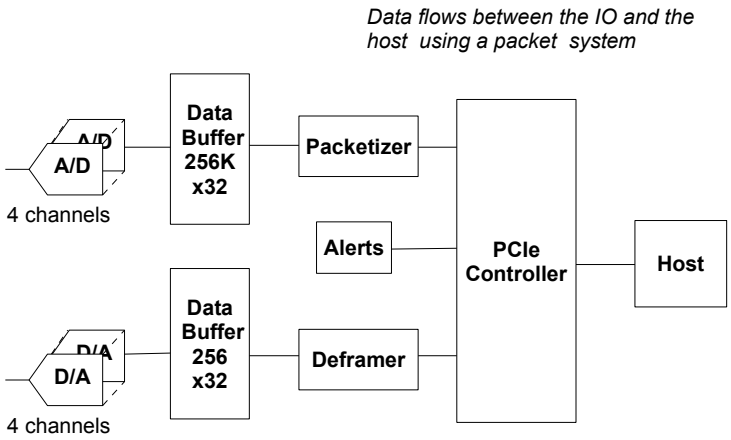


X3-A4D4

Architecture and Features

The analog front end of the X3-A4D4 module has four simultaneously sampling channels of 16-bit, 4 MSPS A/D input, four channels of 50 MSPS, 16-bit D/A converter, and 16 digital IO's. The A/D channels have programmable input ranges and an input bandwidth of 600 kHz. The four DAC channels have a +/-10V output range and an output bandwidth of over 2.5 MHz.

The A/D and DAC channels have been designed with low latency for servo control applications. Latency is <500 ns from the analog input to the usable analog sample in the FPGA . The DAC channels have latency of <400 ns from FPGA to DAC output.



X3-A4D4 Architecture

Controls for triggering and clocks allow precise control over the collection of data. Trigger modes include frames of programmable size, external and software. Multiple X3-A4D4 cards can sample simultaneously using external trigger inputs with synchronized sample clocks. The sample clock can be external or generated from the on-card PLL. The PLL can either use the on-card 100 MHz reference, or can use an external reference. When an external reference is used, the sample clock is synchronous to the reference.

The X3 architecture has data buffering and a packet system to the host that provides an efficient and flexible host interface. The data buffer is a 1M sample SRAM that is used as a dual-queue FIFO, one queue for A/D and one for DACs.. Data to the buffer is transferred to the host using the PCIe controller interface as data packets. The packet data system controls the flow of packets to the host, or other recipient, using a credit-based system managed in cooperation with the host software. The packets may be transmitted continuously for streams of data from the A/Ds or DACs, or as occasional packets for status, controls and analysis results. The data buffering and flow control system delivers high throughput with low latency and complete flexibility for data types and packet sizes to match the application requirements for all types of applications.

The data acquisition process can be monitored using the X3 alert mechanism. The alerts provide information on the timing of important events such as triggering, overranges and thermal overload. Packets containing data about the alert including an absolute system timestamp of the alert, and other information such as current temperature. This provides a precise overview of the card data acquisition process by recording the occurrence of these real-time events making the X3 modules easier to integrate into larger systems.

Software Tools

Software for data logging and analysis are provided with every X3 module. Data can be logged to system memory at full rate or to disk at rates supported by the drive and controller. Triggering, sample rate controls, and data logging features allow you to use X3 modules in your application without ever writing code. Innovative software applications include *Binview* which provides data viewing, analysis and export data to MATLAB for large data files, as well as support applications for logic loading, firmware updates and system configuration.

Software development tools for the X3 modules provide comprehensive support including device drivers, data buffering, card controls, and utilities that allow developers to be productive from the start. At the most fundamental level, the software tools deliver data buffers to your application without the burden of low-level real-time control of the cards. Software classes provide C++ developers a powerful, high-level interface to the card that makes real-time, high speed data acquisition easier to integrate into applications.

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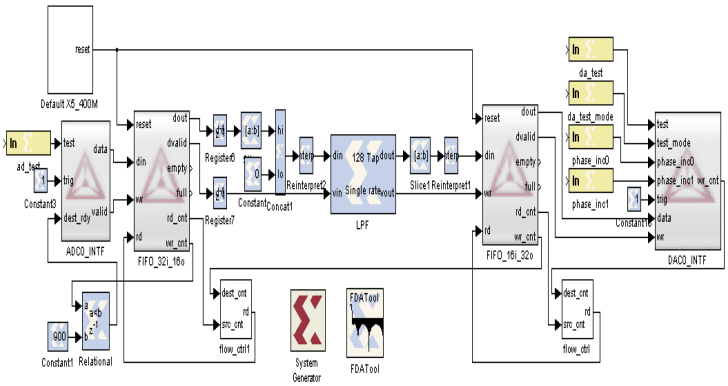
Support for MS Visual C++ is provided. Supported OS include Windows and Linux. For more information, the software tools and on-line help may be downloaded.

Logic Tools

High speed DSP, analysis, customized triggering and other unique features may be added to the X3 modules by modifying the logic. The FrameWork Logic tools support RTL and MATLAB developments. The standard logic provides a hardware interface layer that allows designers to concentrate on the application-specific portions of the design. Designer can build upon the Innovative components for packet handling, hardware interfaces and system functions, the Xilinx IP core library, and third party IP. RTL source for the FrameWork Logic is provided for customization. Each design is provided as a Xilinx ISE project, with a ModelSim testbench illustrating logic functionality.



The MATLAB Board Support Package (BSP) supports logic development using Simulink and Xilinx System Generator. These tools provide a graphical design environment that integrates the logic into MATLAB Simulink for complete hardware-in-the-loop testing and development. The MATLAB tools are an extremely powerful design methodology that can be used to generate, analyze and display the signals in the logic real-time in the system. Once the development is complete, the logic can be embedded in the FrameWork logic using the Xilinx ISE tools.

The FrameWork Logic User sales brochure and User Guide more fully detail the development tools.

Applications Information

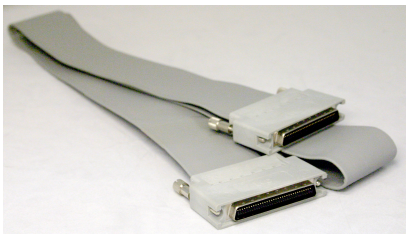
Maximum Data Rates

The maximum data rates supported by the module are limited by the PCI Express transfer rate when the total data rate exceeds 150 MB/s. The PCI Express transfer rate may vary according to the host computer, operating system, and other system activity that may compete for bandwidth. The X3 modules support 250MB/s full duplex during bursts, but actual sustained throughput is 150 MB/s in typical desktop PCs.

It is important to qualify systems for performance when data rates exceeding 150 MB/s are required.

This rate limitation does not apply to data generated in the FPGA.

Cables



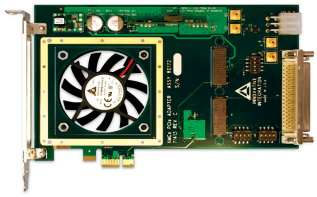
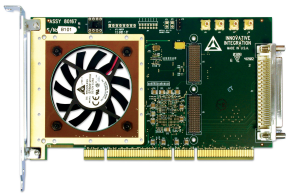
X3 modules uses a shielded, jacketed 68-wire cable assembly for the front panel IO. The pleated copper foil shield cable is “near coax” in its performance. This cable, plus the use of differential signals and use of ground signals as shields, produce the best results. A screw terminal assembly is available.

XMC Adapter Cards

XMC modules can be used in standard desktop system or compact PCI/PXI using an adapter card. The adapter cards are software transparent.

The X3 modules use the auxiliary P16 connector for digital IO and additional clock inputs. A total of 44 bits of digital IO, directly connected to the application FPGA, are routed to the rear edge MDR connector as 22 balanced differential pairs

supporting LVDS or lower speed single-ended LVCMOS signals. The X3 modules also have a sample clock input and PLL reference input to J16. The cPCI/PXI adapter uses these to connect to system clocks, while the PCIe desktop adapter provides SMB input connectors for system clock inputs.

PCIe-XMC Adapter (80172) x1 PCIe to XMC SMB Clock and trigger inputs 	**PCI-XMC Adapter (80167)** 64-bit, 133 MHz PCI-X host x4 PCIe to XMC 	**Compact PCI-XMC Adapter (80207)** 64-bit, 133 MHz PCI-X host x4 PCIe to XMC PXI triggers and clock support 

Applications that need remote or portable IO can use either the eInstrument PC or eInstrument Node with X3 modules.

eInstrument PC with Dual PCI Express XMC Modules (90199) Windows/Linux embedded PC 8x USB, GbE, cable PCIe, VGA High speed x8 interconnect between modules GPS disciplined, programmable sample clocks and triggers to XMCs Up to 400MB/s data logging using FLASH HDD 12V operation 	**eInstrument DAQ Node – Remote IO using cabled PCI Express (90181)** PCI Express system expansion Up to 7 meter cable electrically isolated from host computer software transparent 

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