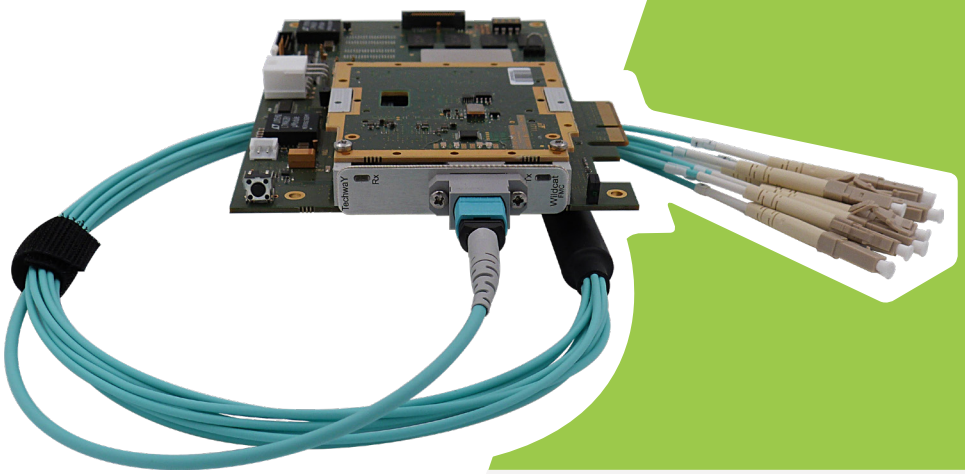
PERSIAN

DEVELOPMENT-BOARD FOR HIGH-SPEED OPTICAL

TECHWAY
SIGNAL VISION SYSTEM

Demo-board for optical component qualification



APPLICATIONS

- Qualification for optical components
- Validation of the optimized network
- Evaluation of the optical budget
- Test-bench setup

BENEFITS

- Ready-to-use :
  - Board and firmware
- User-friendly :
  - Setting parameters for optimization
- Cost-effective
- Protocol agnostic (BERT)

KEY FEATURES

- Multiple links :
  - Up to 4 full duplex links
- Up to 10 Gbps
- Test pattern length : 2^7, 2^{15}, 2^{31}
- Stand-alone
- RADIALL D-Lightsys® Technology

DEFENCE

INDUSTRY

Optical communications have become the new standard in the embedded industry with the increasing demand for bandwidth. This demand is driven by new high-resolution sensors and by intercommunications needed among processing units.

To design, qualify and develop your new systems based on optical, TECHWAY brings you a ready-to-use solution with the PERSIAN development-board.

PERSIAN is a Xilinx Kintex-7 FPGA board which features up to 10 high-speed optical links based Radiall D-Lightsys® technology.

Thanks to its PCIe x4 form factor and its stand-alone capabilities, the PERSIAN can be operated for two main usages :

- Demo-board for the optical component qualification
- Development-board for software and firmware as well as integration purposes

PERSIAN as a demo-board

In this configuration, no need for a PC. PERSIAN is operated in stand-alone in your lab. You just need a JTAG plug and Xilinx WebPACKTM free tool (Serial I/O Analyzer). A built-in BERT firmware is available on board with a wide range of parameter settings to optimize your optical services.

PERSIAN as a development-board

We deliver together with an SDK/driver under Windows and Linux. Once plug into a PC, PERSIAN offers an easy-to-operate development environment for both your firmware and software. To use the PERSIAN as a development board, a Vivado design suite licence is required.

In summary, PERSIAN is ready-to-go, easy-to-use, convenient solution to qualify your optical systems and build test benches.

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PERSIAN FEATURES

- PCIe short form factor format
- PCIe 4 lanes Gen2 (16 Gbps)
- Stand-alone operation mode
- FPGA Kintex-7 (KX 325 or KX 410)
- Up to 4 full duplex links

or

- Up to 10 full duplex links
- Up to 10 Gbps per link
  (user programmable bitrate)
- Front connection : MTP connector
- Commercial temperature range

D-LIGHTSYS® FEATURES

- Proven technology
- Small footprint
- Low consumption
- Qualified for harsh environments
- Wide operating parameters
- Benefits of Radiall's optical interconnect range

ADD-ON PRODUCTS*

- JTAG cable
- Optical cable

* Sold separatly

RELATED PRODUCTS

- PFP-KX7
  - PFP board with Kintex-7 FPGA, PCIe 4x Gen2
- WildcatFMC-4_12
  - VITA 57.1 Optical FMC, 4 full duplex links @12Gbps
- WildcatFMC-12_12
  - VITA 57.4 Optical FMC, 12 full duplex links @12Gbps

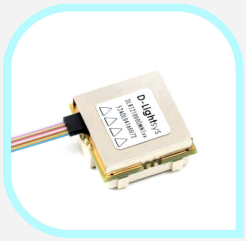
D-LIGHTSYS® TECHNOLOGY

Since 2007, D-Lightsys® transceivers have been flying with military and commercial aircrafts and have proven to be the perfect solution for demanding applications.

The new 10+ G range utilizes D-Lightsys® technology and offers the unique benefits, including a very small footprint and extended link budget for applications where long term data transmission reliability is required. The low power consumption makes these modules especially suited for on board applications (aircraft, UAV, satellites).

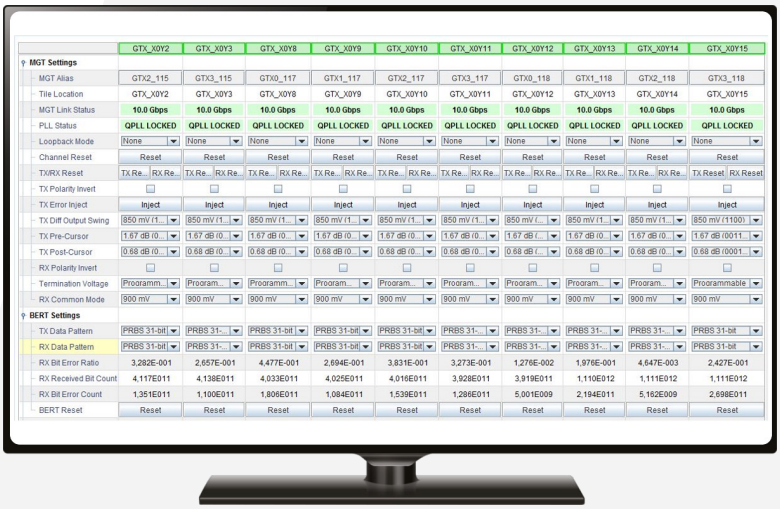
Directly compatible with most digital balanced signal protocols, the 10+ G range meets IEEE std 10G Base-SR10, Fiber Channel, InfiniBand, SFPDP, sRIO and VSR requirements as well as ARINC 818 and DVI video standards.

The D-Lightsys® solutions are qualified for shock and vibration and are in compliance with MIL standards.



D-Lightsys® text and image
ACS 10GB handout - RADIALL

BERT : EASY-TO-USE FIRMWARE



	GTX_X0Y2	GTX_X0Y3	GTX_X0Y8	GTX_X0Y9	GTX_X0Y10	GTX_X0Y11	GTX_X0Y12	GTX_X0Y13	GTX_X0Y14	GTX_X0Y15
MGT Settings										
MGT Alias	GTX2_115	GTX3_115	GTX0_117	GTX1_117	GTX2_117	GTX3_117	GTX0_118	GTX1_118	GTX2_118	GTX3_118
Tile Location	GTX_X0Y2	GTX_X0Y3	GTX_X0Y8	GTX_X0Y9	GTX_X0Y10	GTX_X0Y11	GTX_X0Y12	GTX_X0Y13	GTX_X0Y14	GTX_X0Y15
MGT Link Status	10.0 Gbps	10.0 Gbps	10.0 Gbps	10.0 Gbps	10.0 Gbps	10.0 Gbps	10.0 Gbps	10.0 Gbps	10.0 Gbps	10.0 Gbps
PLL Status	QPLL LOCKED	QPLL LOCKED	QPLL LOCKED	QPLL LOCKED	QPLL LOCKED	QPLL LOCKED	QPLL LOCKED	QPLL LOCKED	QPLL LOCKED	QPLL LOCKED
Loopback Mode	None	None	None	None	None	None	None	None	None	None
Channel Reset	Reset	Reset	Reset	Reset	Reset	Reset	Reset	Reset	Reset	Reset
TX/RX Reset	TX Re...	RX Re...	TX Reset	RX Reset						
TX Polarity Invert										
TX Error Inject	Inject	Inject	Inject	Inject	Inject	Inject	Inject	Inject	Inject	Inject
TX Diff Output Swing	850 mV (1...	850 mV (1...	850 mV (1...	850 mV (1...	850 mV (1...	850 mV (1...	850 mV (...	850 mV (1...	850 mV (1...	850 mV (1100)
TX Pre-Cursor	1.67 dB (0...	1.67 dB (0...	1.67 dB (0...	1.67 dB (0...	1.67 dB (0...	1.67 dB (0...	1.67 dB (...	1.67 dB (0...	1.67 dB (0...	1.67 dB (0011
TX Post-Cursor	0.68 dB (0...	0.68 dB (0...	0.68 dB (0...	0.68 dB (0...	0.68 dB (0...	0.68 dB (0...	0.68 dB (...	0.68 dB (0...	0.68 dB (0...	0.68 dB (0001
RX Polarity Invert										
Termination Voltage	Programm...	Program...	Programm...	Program...	Program...	Program...	Program...	Program...	Program...	Programmable
RX Common Mode	900 mV	900 mV	900 mV	900 mV	900 mV	900 mV	900 mV	900 mV	900 mV	900 mV
BERT Settings										
TX Data Pattern	PRBS 31-bit	PRBS 31-...	PRBS 31-bit	PRBS 31-bit	PRBS 31-bit	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-bit
RX Data Pattern	PRBS 31-bit	PRBS 31-...	PRBS 31-bit	PRBS 31-bit	PRBS 31-bit	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-...	PRBS 31-bit
RX Bit Error Ratio	3,282E-001	2,657E-001	4,477E-001	2,694E-001	3,831E-001	3,273E-001	1,276E-002	1,976E-001	4,647E-003	2,427E-001
RX Received Bit Count	4,117E011	4,138E011	4,033E011	4,025E011	4,016E011	3,928E011	3,919E011	1,110E012	1,111E012	1,111E012
RX Bit Error Count	1,351E011	1,100E011	1,806E011	1,084E011	1,539E011	1,286E011	5,001E009	2,194E011	5,162E009	2,698E011
BERT Reset	Reset	Reset	Reset	Reset	Reset	Reset	Reset	Reset	Reset	Reset

Information and photos subject to change without notice