Atropos

V 1.3 1/29/16

Innovative Integration
... real time solutions!

Precision Sampling Rate Generation and Triggering Controls with High Precision Reference

FEATURES

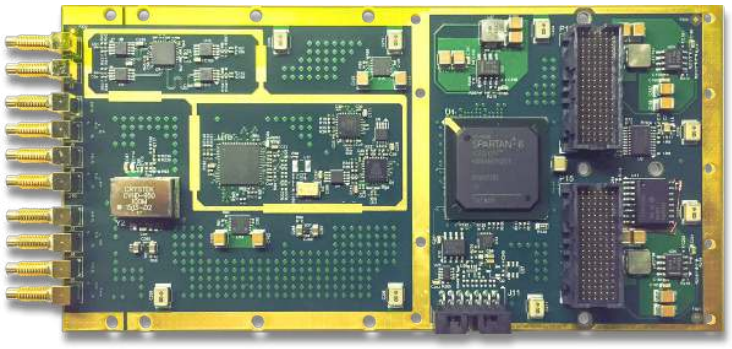
- Clock generation and distribution
- Four single-ended clock outputs*
- External clock/reference input
- Low noise: 135 fs RMS jitter -160 dBc/Hz noise floor (fc=100 MHz)
- Programmable 70.06 to 3080 MHz range
- Onboard 10 MHz, 250 ppb oscilltor or external frequency reference
- Four single-ended trigger outputs
- Supports J16 triggers and local bus
- External trigger input
- XMC Module (75x150 mm)
- PCI Express (VITA 42.3)

APPLICATIONS

- Sample clock generation for high speed data acquisition applications
- Sample clock generation for multi-channel systems
- Synchronization for distributed systems
- Timing Generation

SOFTWARE

- Windows/Linux Drivers
- C++ Host Tools



RoHS 2002/95/EC Compliant

DESCRIPTION

Atropos is an XMC I/O module with precision, low-noise clock generation and distribution for data acquisition and communications timing applications. The module has four output clocks and four output triggers as well as a clock/reference input and a trigger input. The Atropos can also act as a system timing card in multi-board XMC, FMC or PCIe -based systems, providing the reference clock, sample clocks and triggering.

In the sample clock generation mode, Atropos can generate clocks from 70.06 to 3080 MHz. All clock outputs may be referenced to an on-card 280 ppb temperature-compensated oscillator, or an external clock input.

The PLL circuit is fully programmable, providing extremely low noise clocks with 135 fs RMS jitter, -160 dBc/Hz noise floor (fc=100 MHz). The output clocks are phase aligned to within 100 ps. Each output clock is a 1 to 32 subdivision of the external clock or second-stage PLL, which may programmatically operate in either the 2370-2630 or 2920-3080 MHz range.

Windows and Linux applications are provided that are used to configure and control all Atropos features.

Software tools for host development include C++ libraries and drivers for Windows and Linux.

* Differential version available with two clock and two trigger outputs

Atropos

This electronics assembly can be damaged by ESD. Innovative Integration recommends that all electronic assemblies and components circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

Product	Part Number	Description
Atropos	80340-0	PCI Express XMC module with four high-speed single-ended LVPECL clock and synchronous trigger outputs (70-3080 MHz), external trigger and clock inputs, XMC clock support and 280 ppb reference.
	80340-1	PCI Express XMC module with two high-speed differential LVPECL clock and synchronous trigger outputs (70-3080 MHz), external trigger and clock inputs, XMC clock support and 280 ppb reference.
Cables		
SSMC to BNC cable	67156	SSMC to BNC male coax cable, 1m
Adapters		
XMC-PCIe x1 Adapter	80172	PCI Express Carrier card for XMC PCI Express modules, x1 lanes
XMC-PCI Adapter	80167	PCI Carrier card for XMC PCI Express modules, 64-bit PCI-X
XMC-cPCI Adapter	80207	3U Compact PCI Carrier card for XMC PCI Express modules, 64-bit PCI-X
XMC-Cabled PCIe Adapter	90181	Cabled PCI Express Carrier card for XMC PCI Express modules, single-lane.
Embedded PC Host		
eInstrumentPC embedded PC XMC host	90200	Embedded PC with support for two XMC modules; Celeron, Core2Duo or Penryn CPU; Windows or Linux

Atropos

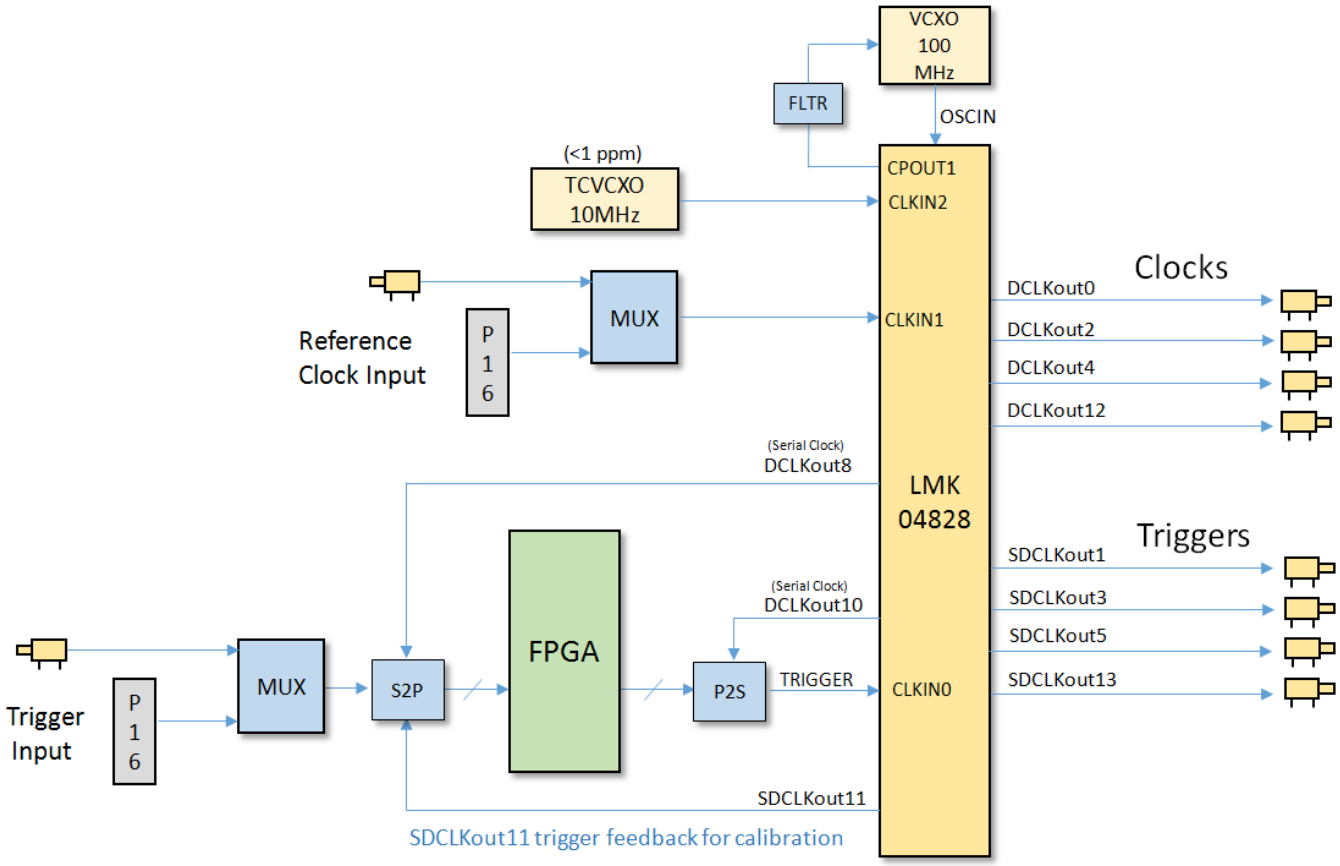


Figure 1. Block Diagram

Atropos

Standard Features

Clock Generation	
Clock Sources	Programmable PLL : TI LMK04828
	External : Sine/Square Input
PLL References	Internal : 10MHz (specs below)
	External : same as external clock
PLL Frequency Range	74.06MHz - 3080MHz
PLL Tuning Resolution	50KHz

Internal PLL Reference	
Frequency	10 MHz
Stability	250 ppb
Accuracy	Calibrated to 1 ppm
Noise	1 Hz: -71 dBc/Hz 10 Hz: -93 dBc/Hz 100 Hz: -117 dBc/Hz 1 KHz: -138 dBc/Hz 10 KHz: -152 dBc/Hz 100 KHz: -155 dBc/Hz

Clock / Reference Inputs	
Inputs (AC coupled)	P16 : Differential LVPECL
	SSMC : Single-ended LVPECL : 800mV p-p LVDS : 400mV p-p LVCMOS : 3.3V p-p
Input Impedance	50 ohm
Frequency	10KHz - 750MHz

Clock Outputs	
Outputs	Single Ended : 4
	Differential : 2
Output Range	800 mVp-p (single-ended), 1.6V p-p differential, min for 50 ohm load
Output Type	LVPECL (single ended / differential)
Output Impedance	50 ohm
Connectors	SSMC female

Triggers	
Modes	Continuous or N-point frame
Sources	Internal (software) External (SSMC / P16)
Output trigger rate	250 MHz max
Frame Sizes	4 to 16M points
External Inputs Software selectable (AC coupled) Note : only 1 source can be selected)	SSMC : Single-ended LVPECL : 800mV p-p LVDS : 400mV p-p LVCMOS : 3.3V p-p
	P16 : Differential LVPECL
Input trigger rise/fall time	100 ps min
Outputs	Single Ended : 4
	Differential : 2
Output Range	800 mVp-p (single-ended), 1.6V p-p differential, min for 50 ohm load
Output Type	LVPECL (single ended / differential)
Output Impedance	50 ohm
Output rise/fall time	< 100 ps typical, depending on loading

ABSOLUTE MAXIMUM RATINGS

Exposure to conditions exceeding these ratings may cause damage!

Parameter	Min	Max	Units	Conditions
Supply Voltage, 3.3V to GND	+3.0	+3.6	V	
Clk / Trigger Input Voltage	0	3.6	V	AC Coupled
Operating Temperature	0	70	C	Non-condensing, forced air cooling required
Storage Temperature	-65	+150	C	
ESD Rating	-	1k	V	Human Body Model
Vibration	-	5	g	9-200 Hz, Class 3.3 per ETSI EN 300 019-1-3 V2.1.2 (2003-04)
Shock	-	40	g peak	Class 3.3 per ETSI EN 300 019-1-3 V2.1.2 (2003-04)

RECOMMENDED OPERATING CONDITIONS

Parameter	Min	Typ	Max	Units
Supply Voltage	+3.15	+3.3	+3.45	V
Operating Temperature	0		60	C

ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range at 0°C to +60°C, unless otherwise noted.

Parameter	Typ	Units	Notes
Output Frequency Range	70.06 - 3080	MHz	
Clock Jitter	91	fs	Target specification with output filter
Accuracy	1	ppm	After calibration
Stability	250	ppb	
Power Consumption	5.8	W	1.76A from 3.3V with 4 outputs @ 400 MHz

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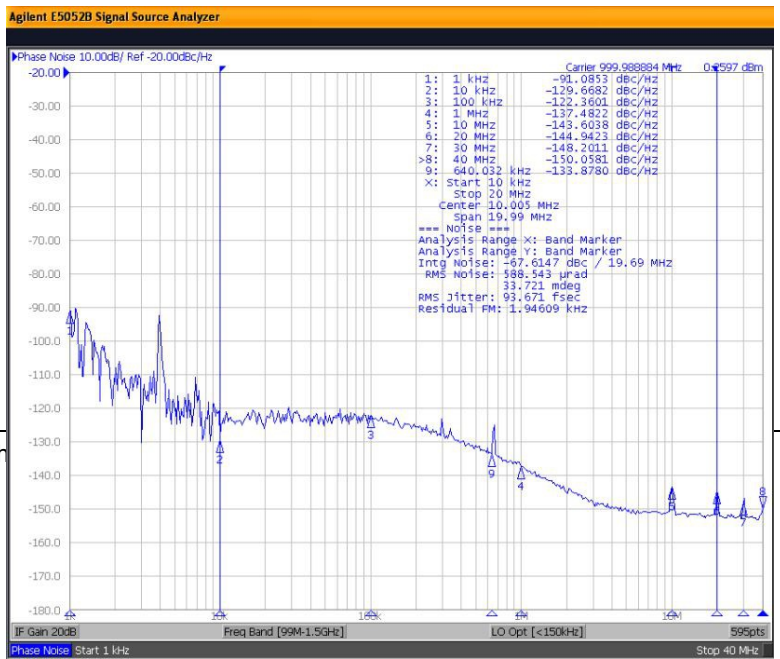
Agilent E5052B Signal Source Analyzer
Phase Noise 10.00dB/ Ref -20.00dBc/Hz
Carrier 99.998887 MHz
1: 1 kHz -110.8660 dBc/Hz
2: 10 kHz -142.6933 dBc/Hz
3: 100 kHz -143.5701 dBc/Hz
4: 1 MHz -155.5058 dBc/Hz
5: 10 MHz -155.9182 dBc/Hz
6: 20 MHz -159.0095 dBc/Hz
7: 30 MHz -160.3667 dBc/Hz
>8: 40 MHz -159.8492 dBc/Hz
9: 640.032 kHz -152.8927 dBc/Hz
X: Start 10 kHz
Stop 20 MHz
Center 10.005 MHz
Span 19.99 MHz
=== Noise ===
Analysis Range X: Band Marker
Analysis Range Y: Band Marker
Intg Noise: -84.4362 dBc / 19.69 MHz
RMS Noise: 84.8601 µrad
4.86213 mdeg
RMS Jitter: 135.061 fsec
Residual FM: 691.727 Hz
IF Gain 20dB
Freq Band [99M-1.5GHz]
LO Opt [<150kHz]
595pts
Phase Noise
Start 1 kHz
Stop 40 MHz


Agilent E5052B Signal Source Analyzer
Phase Noise 10.00dB/ Ref -20.00dBc/Hz
Carrier 999.988884 MHz
1: 1 kHz -91.0853 dBc/Hz
2: 10 kHz -129.6682 dBc/Hz
3: 100 kHz -122.3601 dBc/Hz
4: 1 MHz -137.4822 dBc/Hz
5: 10 MHz -143.6038 dBc/Hz
6: 20 MHz -144.9423 dBc/Hz
7: 30 MHz -148.2011 dBc/Hz
>8: 40 MHz -150.0581 dBc/Hz
9: 640.032 kHz -133.8780 dBc/Hz
X: Start 10 kHz
Stop 20 MHz
Center 10.005 MHz
Span 19.99 MHz
=== Noise ===
Analysis Range X: Band Marker
Analysis Range Y: Band Marker
Intg Noise: -67.6147 dBc / 19.69 MHz
RMS Noise: 588.543 µrad
33.721 mdeg
RMS Jitter: 93.671 fsec
Residual FM: 1.94609 kHz
IF Gain 20dB
Freq Band [99M-1.5GHz]
LO Opt [<150kHz]
595pts
Phase Noise
Start 1 kHz
Stop 40 MHz

Atropos

Architecture and Features

The Atropos module is a PCI Express XMC module designed to support high speed digitizing systems with multiple channels. The card provides extremely low noise clock signals that are required for accurate digitizing of high speed analog signals in systems such as RF/IF front ends, RADAR systems and high speed pulse digitizing.

Distributed systems are supported using an external reference, often supplied via GPS or IEEE1588, allowing systems to be tightly locked to world time without physically sharing any signals.

Clock Generation

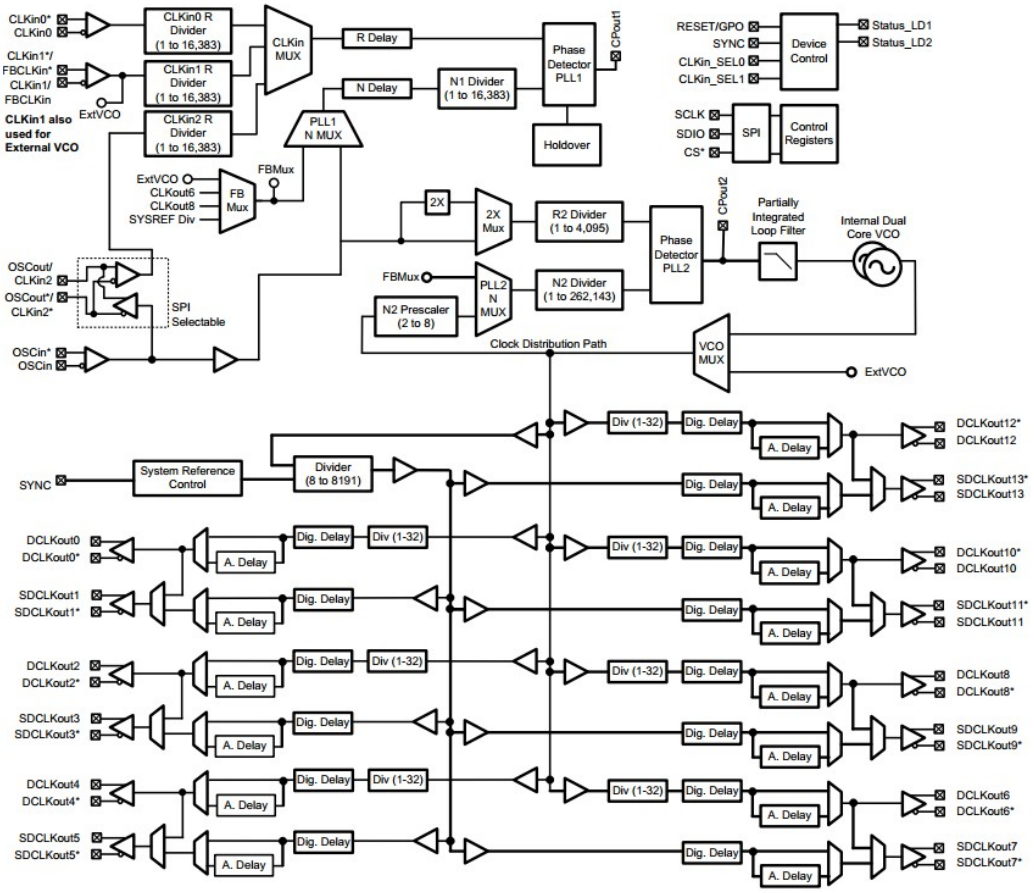


Figure 4. LMK04828 PLL Block Diagram

Atropos features a flexible sample rate generation architecture built around a dual stage PLL with tunable VCXO. The PLLs and VCXOs are fully programmable with an output range from 70.06 to 3080 MHz as shown in the block diagram below.

The PLL reference inputs are also software programmable and provide selection between a 10 MHz reference oscillator, or an external input. The reference oscillator is offered with 0.25 ppm temp-stability rating. The references may be divided before the PLL by values from 1 to 16383 (not all numbers inclusive) so that high frequency external reference inputs can be used.

Atropos

Clock Outputs

There are four clock outputs on the front panel and one J16 XMC clocks. All clock outputs may be synchronous or individually subdivided from the PLL or external clock, or the reference clock.

Triggering

Atropos has four trigger outputs to the front panel and an triggers for J16. The triggers are programmable for framed mode, used for data snapshots, or continuous mode. The trigger can be fired from software, external input, or GPS time. All trigger outputs are synchronous.

Trigger Mode	Continuous	*Trigger is true on next rising edge of the sample clock until source is deasserted*
	Framed	*Once fired, the trigger is true for N data points*

PLL Range Limitations

The figure below shows the ranges of frequencies available for each divider ratio applied to the VCO ranges.

The IC has two VCO's, with slightly different frequency ranges, shown at the top of each column. The table shows the frequency ranges resulting from each divider ratio applied to the VCO's. In addition there are indicators of how to shift to the next range to get increasing frequencies (arrow indicates which VCO, number indicates rows to go up or down). The yellow shaded cells show where the next higher available frequency leaves a hole. The red shaded cells show ranges that would not typically be used because the range is completely contained within a range available by using the other VCO. It is possible that the red ranges might be used if there are idiosyncrasies that cause unusual "sweet spots".

For lower frequencies, it appears that VCO0 would be used.

The IC also has a second "System Reference" frequency path that allows higher divider ratios (8 to 8191) which allow lower frequencies to be generated. The last row of cells show the frequencies that result with this divider set at 8191.

Atropos

VCO Range MHz	2370.000	2630.000		2920.000	3080.000		1840.000	1970.000		2440.000	2505.000	
Divider ratio												
1	2370.000	2630.000	>	2920.000	3080.000		1840.000	1970.000	>	2440.000	2505.000	
2	1185.000	1315.000	>	1460.000	1540.000	<1	920.000	985.000	>	1220.000	1252.500	<1
3	790.000	876.667	>	973.333	1026.667	<1	613.333	656.667	>	813.333	835.000	<1
4	592.500	657.500	>	730.000	770.000	<1	460.000	492.500	-1>	610.000	626.250	<1
5	474.000	526.000	>	584.000	616.000	<1	368.000	394.000	-1>	488.000	501.000	^
6	395.000	438.333	-1>	486.667	513.333	<1	306.667	328.333	-1>	406.667	417.500	<2
7	338.571	375.714	-1>	417.143	440.000	<2	262.857	281.429	-1>	348.571	357.857	<2
8	296.250	328.750	-1>	365.000	385.000	<2	230.000	246.250	-2>	305.000	313.125	<2
9	263.333	292.222	-1>	324.444	342.222	<2	204.444	218.889	-2>	271.111	278.333	
10	237.000	263.000	^	292.000	308.000	<2	184.000	197.000	-2>	244.000	250.500	<3
11	215.455	239.091	^	265.455	280.000		167.273	179.091	^	221.818	227.727	<3
12	197.500	219.167	^	243.333	256.667		153.333	164.167	-3>	203.333	208.750	<3
13	182.308	202.308	^	224.615	236.923		141.538	151.538	-3>	187.692	192.692	
14	169.286	187.857	^	208.571	220.000		131.429	140.714	^	174.286	178.929	
15	158.000	175.333	^	194.667	205.333		122.667	131.333	-4>	162.667	167.000	<4
16	148.125	164.375	^	182.500	192.500		115.000	123.125	^	152.500	156.563	<4
17	139.412	154.706	^	171.765	181.176		108.235	115.882	^	143.529	147.353	
18	131.667	146.111	^	162.222	171.111		102.222	109.444	^	135.556	139.167	
19	124.737	138.421	^	153.684	162.105		96.842	103.684	^	128.421	131.842	<5
20	118.500	131.500	^	146.000	154.000	<4	92.000	98.500	^	122.000	125.250	
21	112.857	125.238	^	139.048	146.667	^	87.619	93.810	^	116.190	119.286	<5
22	107.727	119.545	^	132.727	140.000	^	83.636	89.545	^	110.909	113.864	<5
23	103.043	114.348	^	126.957	133.913	^	80.000	85.652	^	106.087	108.913	<5
24	98.750	109.583	^	121.667	128.333	^	76.667	82.083	^	101.667	104.375	<6
25	94.800	105.200	^	116.800	123.200	^	73.600	78.800	^	97.600	100.200	<6
26	91.154	101.154	^	112.308	118.462	^	70.769	75.769	^	93.846	96.346	<6
27	87.778	97.407	^	108.148	114.074	^	68.148	72.963	^	90.370	92.778	<7
28	84.643	93.929	^	104.286	110.000	^	65.714	70.357	^	87.143	89.464	<7
29	81.724	90.690	^	100.690	106.207	^	63.448	67.931	^	84.138	86.379	<7
30	79.000	87.667	^	97.333	102.667	^	61.333	65.667	^	81.333	83.500	<7
31	76.452	84.839	^	94.194	99.355	^	59.355	63.548	^	78.710	80.806	<8
32	74.063	82.188	^	91.250	96.250	^	57.500	61.563	^	76.250	78.281	<8
Frequencies above are available at DCLKout or SDCLKout												
Reference Divider allows lower frequencies, down to frequencies shown (at SDCLKout only)												
8191	0.289	0.321		0.356	0.376		0.225	0.241		0.298	0.306	

Distributed Data Acquisition

The external reference is used for distributed applications so that sample clocks can be synchronous to allow creation of wide channel count applications. Typically, a GPS reference clock is used if systems are located in diverse geographic locations whereas an IEEE1588 reference is used if the system elements are connected via a dedicated local network.

Software Tools

Atropos can be easily configured using the supplied example program. The application provides a control panel interface for configuring the PLL and clock distribution features including reference source, output frequency, triggering modes, and XMC timing. No custom development is necessary for most applications. Configurations may be saved for instant recall, or stored and recalled later.

Software development tools for Atropos provides comprehensive support including device drivers, card controls, and utilities that allow developers to be productive from the start. Software classes provide C++ developers a powerful, high-level interface to the card making the Atropos easier to integrate into applications.

Support for MS Visual C++ and GNU C++ is provided. Supported OS include Windows and Linux. For more information, the software tools User Guide and on-line help may be downloaded.

Atropos

Applications Information

Cables

The Atropos module uses coaxial cable assemblies for the IO. The mating cables have an SSMC male connector and 50 ohm characteristic impedance for best signal quality.

XMC Adapter Cards

XMC modules can be used in standard desktop system or compact PCI/PXI using a XMC adapter card. An auxiliary power connector to the PCI Express adapters provides additional power capability for XMC modules when the slot is unable to provide sufficient power. The adapter cards allow the XMC modules to be used in any PCIe or PCI system.

Atropos uses the auxiliary P16 connector to provide an additional trigger and clock input, if provided by the XMC adapter. Like the SSMC connector inputs, internal biasing tolerates unconnected inputs from P16.

Refer to the Atropos Hardware Manual for complete P15/P16 pinouts.

PCIe-XMC Adapter (80172) x1 PCIe to XMC Clock and trigger inputs	**PCIe-XMC Adapter x8 lane (80173)** x8 PCIe to XMC x8 RIO ports supported on P16	**PCI-XMC Adapter (80167)** 64-bit, 133 MHz PCI-X host x4 PCIe to XMC	**Compact PCI-XMC Adapter (80207)** 64-bit, 133 MHz PCI-X host x4 PCIe to XMC PXI triggers and clock support
			

Applications that need remote or portable IO can use either the eInstrument PC or eInstrument Node with X3 modules.

Atropos

eInstrument PC with Dual PCI Express XMC Modules (90200)

Windows/Linux embedded PC
Powerful i7 CPU e
8x USB, GbE, cable PCIe, VGA
High speed x8 interconnect between modules
GPS disciplined, programmable sample clocks and triggers to XMCs
800 MB/s, 2 TB datalogger
12V operation

eInstrument DAQ Node – Remote IO using cabled PCI Express (90181)

PCI Express system expansion
Up to 7 meter cable
electrically isolated from host computer
software transparent

Atropos

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