X6-400M

V2.0 05/22/18

Innovative Integration
a **molex** company

XMC Module with Two 400/500 MSPS A/Ds, Two 500 MSPS DACs, Xilinx Virtex-6 FPGA, 4 GB LPDDR2

FEATURES

- Two 400 MSPS, 14-bit A/D channels (500MSPS, 12-bit option)
- Two 500 MSPS, 16-bit D/A channels
- Xilinx Virtex-6 SX475T/SX315T/LX240T
- 4 banks of 1 GB DRAM (4 GB total)
- Ultra-low jitter programmable clock
- Gen2 x8 PCI Express providing 3.2 GB/s sustained transfer rates (-2 FPGA Required)
- Digital IO: 32-bits LVDS/64-bit LVCMOS
- XMC module (75x150 mm)
- 22 – 28 W typical
- Conduction cooling per VITA 20
- Ruggedization Levels for wide temperature and Vibration/Shock
- CE and FCC certified
- Adapters for VPX, Compact PCI, desktop PCI and cabled PCI Express systems

APPLICATIONS

- Wireless Receiver and Transmitter
- LTE, WiMAX Physical Layer
- RADAR
- Medical Imaging
- High Speed Data Recording and Playback
- IP development

SOFTWARE

- MATLAB/VHDL FrameWork Logic
- Windows/Linux/VxWorks Drivers
- C++ Host Tools

XILINX®

MATLAB®

RoHS 2002/95/EC Compliant

X6 400m

DESCRIPTION

The X6-400M integrates high speed digitizing and signal generation with signal processing on a PMC/XMC IO module with a powerful Xilinx Virtex 6 FPGA signal processing core, and high performance PCI Express/PCI host interface.

The X6-400M features two 14-bit 400MSPS or 12-bit 500 MSPS A/Ds, either AC or DC-coupled, plus two 500MSPS update rate DACs. The DAC can be used a single 1 GHz output channel. Analog IO is either AC or DC coupled. Receiver IF frequencies of up to 250 MHz are supported. The sample clock is from either a low-jitter PLL or external input. Multiple cards can be synchronized for sampling.

A Xilinx Virtex6 LX240T (LX315T and SX475T options) with 4 banks of 1 GB DRAM provides a very high performance DSP core with over 2000 MACs (SX315T). The close integration of the analog IO, memory and host interface with the FPGA enables real-time signal processing at extremely high rates.

The X6-400M power consumption is 19W for typical operation. The module may be conduction cooled using VITA20 standard and a heat spreading plate. Ruggedization levels for wide-temperature operation from -40 to +85C operation and 0.1 g^2/Hz vibration. Conformal coating is available.

The FPGA logic can be fully customized using VHDL and MATLAB using the Frame Work Logic tool set. The MATLAB BSP supports real-time hardware-in-the-loop development using the graphical block diagram Simulink environment with Xilinx System Generator. IP cores for many wireless and DSP functions such as DDC, PSK/FSK demod, OFDM receiver, correlators and large FFT are available.

Software tools for host development include C++ libraries and drivers for Windows, Linux and VxWorks. Application examples demonstrating the module features are provided.

X6-400M

	This electronics assembly can be damaged by ESD. Innovative Integration recommends that all electronic assemblies and components circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

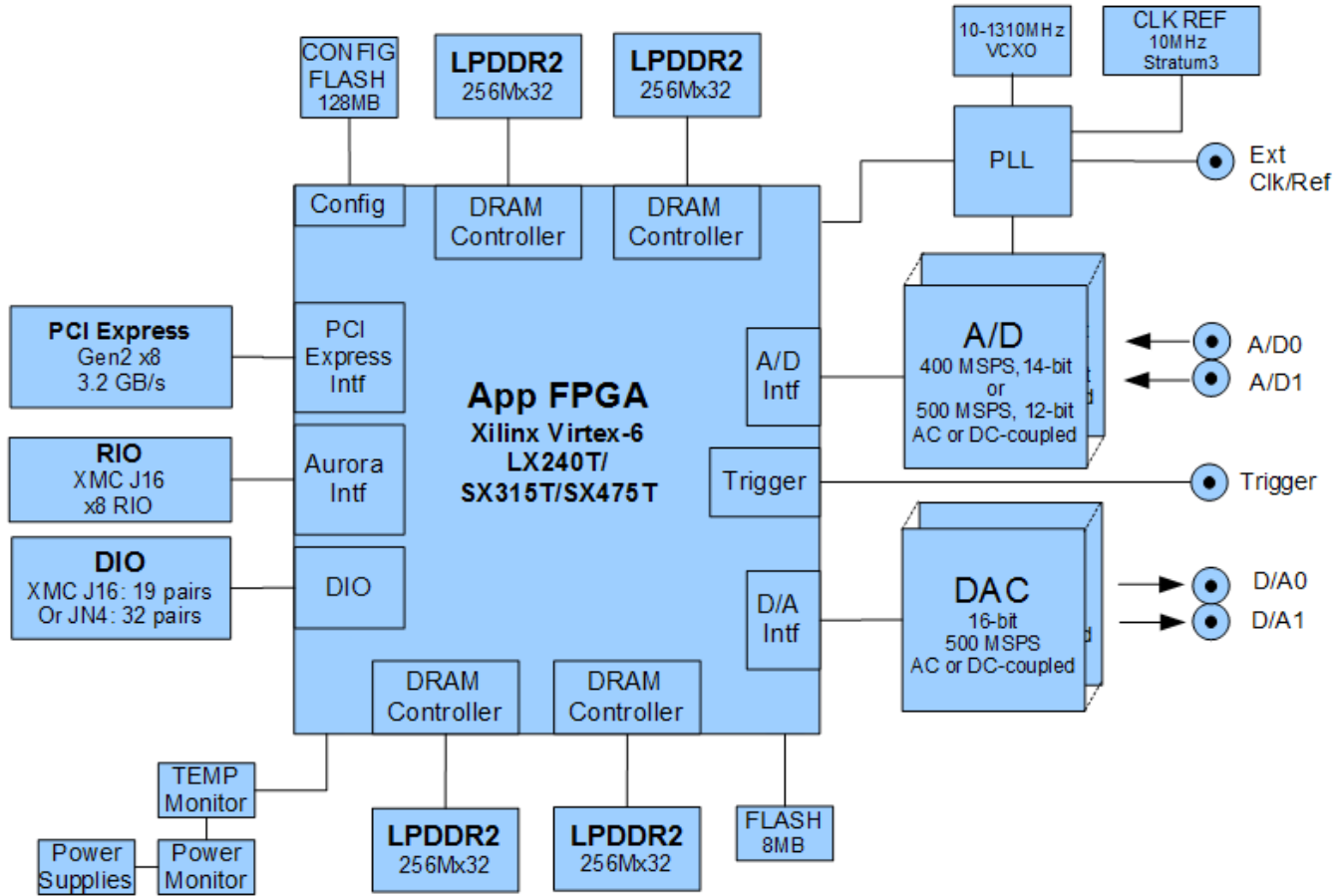| Product	Part Number	Description
X6-400M	80270-<CFG>-<ER>	PMC/XMC module with two 400 MSPS, 14-bit A/Ds, two 500 MSPS DACs, Virtex-6 FPGA, 4GB DRAM <CFG> is Configuration. 0: LX240T1, Gen1, DC-Coupled A/D, DC-Coupled DAC; 1: SX315T1, Gen1, DC-Coupled A/D, DC-Coupled DAC; 2: LX240T2, Gen2, AC-Coupled A/D, AC-Coupled DAC; 3: LX240T2, Gen2, AC-Coupled A/D, AC-Coupled DAC; 4: LX240T1, Gen1, AC-Coupled A/D, AC-Coupled DAC; 5: SX315T1, Gen1, AC-Coupled A/D, AC-Coupled DAC; 6: LX240T2, Gen2, DC-Coupled A/D, DC-Coupled DAC; 7: SX475T1, Gen1, DC-Coupled A/D, DC-Coupled DAC; 8: SX475T2, Gen2, DC-Coupled A/D, DC-Coupled DAC; 9: SX475T1, Gen1, AC-Coupled A/D, AC-Coupled DAC; 10: SX475T2, Gen2, AC-Coupled A/D, AC-Coupled DAC; 11: SX315T2, Gen2, AC-Coupled A/D, AC-Coupled DAC; 12: SX315T2, Gen2, DC-Coupled A/D, DC-Coupled DAC; <ER> is environmental rating **L0...L4**.
Logic Development Package		
X6-400M FrameWork Logic	55034	X6-400M FrameWork Logic board support package for RTL and MATLAB. Includes technical support for one year.
Cables		
SMA to BNC cable	67048	IO cable with SMA (male) to BNC (female), 1 meter
Adapters		
XMC-PCIe Adapter	80259	PCI Express carrier card for XMC PCI Express modules, x8 lanes. Preferred for X6 modules.
XMC-PCIe Adapter	80172-0	PCI Express carrier card for XMC PCI Express modules, x1 lanes
XMC-PCI Adapter	80167-0	PCI carrier card for XMC PCI Express modules, 64-bit PCI
XMC-Compact PCI/PXI Adapter	80207	3U compact PCI carrier card for XMC PCI Express modules, 64-bit PCI. Support for PXI clock and trigger features (logic dependent).
Remote Enclosure	90181	Cabled PCI Express Carrier card for XMC PCI Express modules, single-lane.
VPX Adapter	80262	3U VPX adapter for X6. Air-cooled or conduction-cooled versions. REDI covers available.
Embedded Computer Hosts		

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eInstrument-PC embedded PC XMC host	90200	Embedded PC with support for two XMC modules; Intel i7 CPU; Windows, Linux
eInstrument-PC-Atom low-power embedded PC XMC host	90201	Embedded PC with support for two XMC modules; Intel Atom or i7 CPU; Windows, Linux
VPXI-ePC: 3U VPX PC with 4 expansion slots	90271	3U VPX embedded PC with 4 expansion slots, integrated timing and data plane; Intel i7 CPU; Windows, Linux
Heatsinks		
Standard Adapter (VPX, PXIe, DAQ-Node, eInstrument-PC, XMC-PCIe Adapter)	61548-1	Assembly, Heatsink Hardware, X6, XA on PXIe, VPX, ePC, DAQ-Node, XMC-PCIe Adapter
Standard Adapter (ePC-Duo)	Not Needed	EPC-Duo has the correct heatsinks installed.
Standard Adapter (SBC-Nano)	61543-1	Assembly, Heatsink Hardware, X6, XA on ePC-Nano

Figure 1. Block diagram

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X6-400M Block Diagram

CONFIG FLASH 128MB

LPDDR2 256Mx32

LPDDR2 256Mx32

10-1310MHz VCXO

CLK REF 10MHz Stratum3

Config

DRAM Controller

DRAM Controller

PLL

Ext Clk/Ref

PCI Express Gen2 x8 3.2 GB/s

PCI Express Intf

App FPGA Xilinx Virtex-6 LX240T/ SX315T/SX475T

A/D Intf

A/D 400 MSPS, 14-bit or 500 MSPS, 12-bit AC or DC-coupled

A/D0

A/D1

RIO XMC J16 x8 RIO

Aurora Intf

Trigger

Trigger

DIO XMC J16: 19 pairs Or JN4: 32 pairs

DIO

D/A Intf

DAC 16-bit 500 MSPS AC or DC-coupled

D/A0

D/A1

DRAM Controller

DRAM Controller

TEMP Monitor

Power Supplies

Power Monitor

LPDDR2 256Mx32

LPDDR2 256Mx32

FLASH 8MB

Operating Environment Ratings

X6 modules rated for operating environment temperature, shock and vibration are offered. The modules are qualified for wide temperature, vibration and shock to suit a variety of applications in each of the environmental ratings L0 through L4 and 100% tested for compliance. Click this link "Ruggedization Levels" to see the Ruggedization Levels available.

Minimum lot sizes and NRE charges may apply. Contact sales support for pricing and availability.

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Standard Features

Analog Input	
Inputs	2
Input Range	2 Vp-p (DC-coupled) 2.2 Vp-p (AC-coupled)
Input Type	Single ended, AC or DC coupled
Input Impedance	50 ohm
A/D Device	Texas Instruments ADS5474 (400MSPS, 14-bit) Texas Instruments ADS5463 (500MSPS, 12-bit)
A/D Resolution	14-bit or 12-bit
A/D Sample Rate	20 MHz to 400 MHz (400MSPS version) 20 MHz to 500 MHz (500MSPS version)
Input Bandwidth	5 MHz to 1000 MHz (-3dB) (AC-Coupled) DC to 250 MHz (-3dB) (DC-Coupled)

Analog Output	
Outputs	2
Output Range	0.9 Vp-p (AC-Coupled) 1 Vp-p (DC-Coupled)
Output Type	Single ended, AC or DC coupled
Output Impedance	50 ohm
DAC Device	Texas Instruments DAC5682Z
DAC Resolution	16-bit
DAC Update Rate	1000 MHz max, single channel mode; 500 MHz max, dual channel mode
Interpolation	None, 2x, 4x
Output Bandwidth	5 MHz to 350 MHz (-3dB) (AC-Coupled) 220 MHz (-3dB) (DC-Coupled)

FPGA	
Device	Xilinx Virtex-6
Speed Grade	-1 or -2
Size	SX315T: ~31M gate equivalent
Flip-Flops	SX315T: 393K
Multipliers	SX315T: 1,344
Slice	SX315T: 49,200
Block RAMs	SX315T: 1,408 (25344 Kbits)
Rocket IO	16 lanes @ 5 Gbps (-1 speed)
Configuration	JTAG or FLASH In-system reprogrammable

Memories	
DRAM Size	4 GB; 4 banks of 1 GB each
DRAM Type	LPDDR2 DRAM
DRAM Controller	Controller for DRAM implemented in logic. DRAM is controlled as a single bank.
DRAM Rate	Up to 5.2 GB/s sustained transfer rate per bank (333 MHz clock)

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Host Interface	
PCI Express	x8 Lanes, VITA 42.3 PCI Express Gen 2 (x4 for -1 speed FPGA, x8 for -2 speed FPGA)
PCI Express Sustained Rate	3.2 GB/s (Gen2 x8) 1.2 GB/s (Gen2 x4 or Gen1 x8)

Clocks and Triggering	
Clock Sources	PLL or External
	0.3125 to 1000 MHz on-board PLL, external input is 0.1 Vp-p to 3.3 Vp-p, AC-Coupled, 50 ohm
PLL Reference	External or 10 MHz on-board 10 MHz ref is +/-250 ppb -40 to 85 C
PLL Resolution	100 kHz Tuning Resolution
Phase Noise	-130 dBc @ 100 kHz
Triggering	External, software, acquire N frame
Ext Trigger Timing	Risetime < 1.0 uS
Ext Trigger Level	0.5 – 2.5 Vp-p
Decimation	1:1 to 1:4095 in FPGA
Channel Clocking	All channels are synchronous
Multi-card Synchronization	External triggering input is used to synchronize sample clocks or an external clock and trigger may be used.
Latency	A/D: 36.5 fs cycles DAC: 94 fs cycles

Monitoring	
Alerts	Trigger Start, Trigger Stop, Queue Overflow, Channel Over-range, Timestamp Rollover, Temperature Warning, Temperature Failure
Alert Timestamping	5 ns resolution, 32-bit counter

Application IO (J4/J16)	
Rocket IO Channels	8 (J16)
Rocket IO data rate	5 Gbps/lane (4 Gbps effective rate when 8b/10b encoded)
DIO Bits, total	32 (J16/J4)
Signal Standard	LVCMOS (2.5V) – NOT 3.3 compatible
Drive	+/-12 mA
Connectors	PMC J4/XMC J16

Power	
Consumption	22W (VPWR = 5V, 2 DDR banks and no Aurora ports instantiated, 4 lane PCIe) 28W (VPWR = 12V, 4 DDR banks, all Aurora ports, 4 lane PCIe)
Temperature Monitor	Software with programmable alarms
Over-temp Monitor	Disables power supplies
Power Control	Channel enables and power up enables
Heat Sinking	Conduction cooling supported (VITA20 subset)

Physicals	
Form Factor	Single width IEEE 1386 Mezzanine Card
Size	75 x 150 mm
Weight	130g
Hazardous Materials	Lead-free and RoHS compliant

Certifications	
CE (European Standards)	EN55022: 2006 + A1 : 2007 EN 61000-3-3: 1995 +A1: 2001 & A2 : 2005 EN 61000-3-2: 2006 EN 55024: 1998 + A1: 2001 & A2: 20003
FCC (USA)	Class B

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ELECTRICAL CHARACTERISTICS			
Over recommended operating free-air temperature range at 0°C to +60°C, unless otherwise noted.			
Parameter	Typ	Units	Notes
A/D Channels			
Analog Input Bandwidth	250	MHz	-3dB, DC coupled inputs
	1000	MHz	-3dB, AC coupled inputs
Analog Input Passband Flatness	0.5	dB	0 to 100 MHz, DC coupled
	0.3	dB	0 to 200 MHz, AC coupled
Broadband SFDR	69	dB	Fin = 70.1 MHz, 95% FS, sine sampled at 400 MSPS; Broadband DC to 200 MHz, DC coupled
	79	dB	Fin = 70.1 MHz, 95% FS, sine sampled at 400 MSPS; Broadband DC to 200 MHz, AC coupled
SFDR, 70 MHz Carrier +/-5 MHz Band	90	dB	Fin = 70.1 MHz, 95% FS, sine sampled at 400 MSPS; Broadband DC to 200 MHz, DC coupled
	95	dB	Fin = 70.1 MHz, 95% FS, sine sampled at 400 MSPS; Broadband DC to 200 MHz, AC coupled
Harmonic Distortion	58	dB	Fin = 70.1 MHz, 95% FS, sine sampled at 400 MSPS; Broadband DC to 200 MHz, DC coupled
	82.1	dB	Fin = 70.1 MHz, 95% FS, sine sampled at 400 MSPS; Broadband DC to 200 MHz, AC coupled
ENOB	10.1	bits	Fin = 70.1 MHz, 95% FS, sine sampled at 400 MSPS; Broadband DC to 200 MHz, DC coupled
	10.9	bits	Fin = 70.1 MHz, 95% FS, sine sampled at 400 MSPS; Broadband DC to 200 MHz, AC coupled
S/N	62.7	dB	Fin = 70.1 MHz, 95% FS, sine sampled at 400 MSPS; Broadband DC to 200 MHz, DC coupled
	67.3	dB	Fin = 70.1 MHz, 95% FS, sine sampled at 400 MSPS; Broadband DC to 200 MHz, AC coupled
Crosstalk	- 91/ - 100	dB	Measured channel grounded with a 101 MHz, 95% FS sine input on other channel (DC/AC coupled)
Noise Floor	-100	dB	Fin = 70 MHz, 95% FS, sine sampled at 400 MSPS; Broadband DC to 200 MHz, AC coupled
	-105	dB	Fin = 70 MHz, 95% FS, sine sampled at 400 MSPS; Broadband DC to 200 MHz, AC coupled
Offset Error	< 500	μV	Factory calibration, average of 64K samples after warm-up.
Gain Error	< 0.2	%	Factory calibration after warm-up.

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ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range at 0°C to +60°C, unless otherwise noted.

| Parameter	Typ	Units	Notes
DAC Channels			
Analog Output Range	+/- 450	mV	Typical, AC coupled
	+/- 500	mV	Typical, DC coupled
Analog Output Bandwidth	220	MHz	DC coupled, no sin(x)/x compensation
	350	MHz	AC coupled, no sin(x)/x compensation
Output Amplitude Variation	0.7	dB	0 – 100 MHz, DC coupled, no sin(x)/x compensation
	0.8	dB	1 – 100 MHz, AC coupled, no sin(x)/x compensation
SFDR	66	dB	70.1 MHz sine output, 0 dBFS, AC coupled
	50	dB	70.1 MHz sine output, 0 dBFS, DC coupled
S/N	59.7	dB	70.1 MHz sine output, 0 dBFS, AC coupled
	58	dB	70.1 MHz sine output, 0 dBFS, DC coupled
THD	-62	dB	70.1 MHz sine output, 0 dBFS, AC coupled
	-49	dB	70.1 MHz sine output, 0 dBFS, DC coupled
Inter-modulation Distortion	< -75	dB	70 +/- 0.5 MHz, -6 dBFS, AC coupled
Noise floor	-100	dB	AC or DC output
Gain Error	< 0.02	% of FS	Calibrated
Offset Error	< 10	mV	Calibrated

RELIABILITY

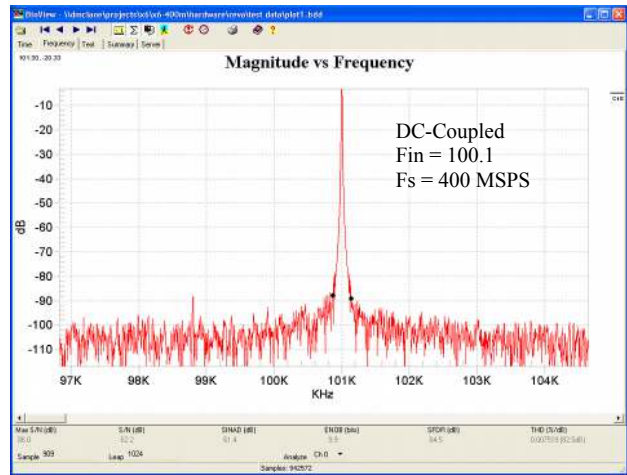|	
Failures/Million Hours	10.31
MTBF	96949.6 Hours

Note: Reliability data is based on normal enviromental conditions operating at and temperature of 50C.
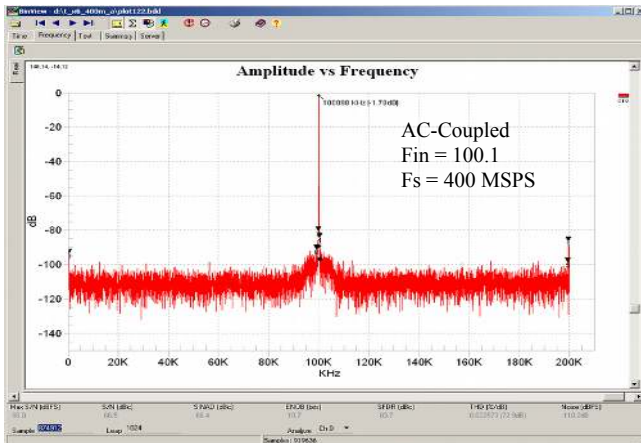
X6-400M
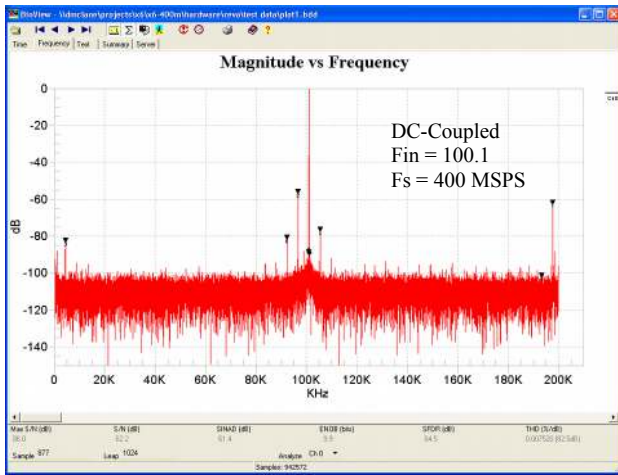
DC-Coupled A/D wideband signal quality, Fin = 101 MHz, Fs = 400 MHz on-board PLL. Channel 0, 15 pF parallel cap at A/D device inputs

DC-Coupled A/D narrowband signal quality, Fin = 101 MHz, Fs = 400 MHz on-board PLL. Channel 0, 15 pF parallel cap at A/D device inputs
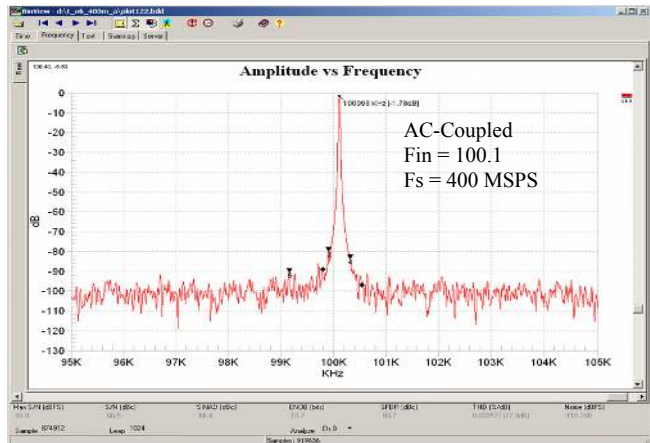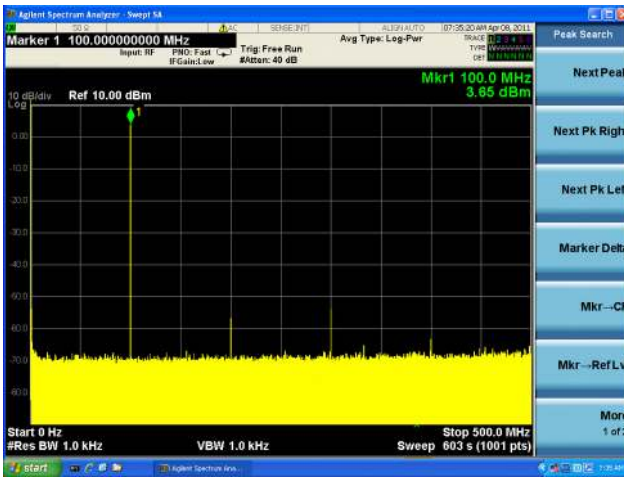

AC-Coupled A/D wideband signal quality, Fin = 100.1 MHz, Fs = 400 MHz on-board PLL. Channel 0, 2.2 pF parallel cap at A/D device inputs
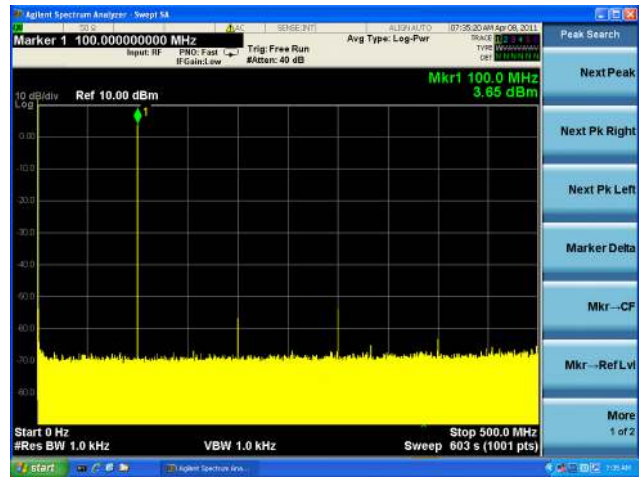

AC-Coupled A/D narrowband signal quality, Fin = 101 MHz, Fs = 400 MHz on-board PLL. Channel 0, 15 pF parallel cap at A/D device inputs

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DC-Coupled output signal quality for Fout = 100.1 MHz, Fs = 1 GSPS.

AC-Coupled output signal quality for Fout = 100.1 MHz, Fs = 1 GSPS.

Architecture and Features

The X6-400M module architecture integrates analog IO with an FPGA computing core, memories and PCI host interface. This architecture tightly couples the FPGA to the analog and enables the module to perform real-time signal processing with low latency and extremely high rates making it ideal as a front-end for demanding applications in wireless, RADAR and medical imaging applications.

Analog IO

The analog front end of the X6-400M module has two simultaneously sampling channels of 14-bit, 400MSPS or 12-bit 500 MSPS A/D input. The A/D inputs have an analog input bandwidth of up to 400 MHz for wideband and direct sampling applications. The A/Ds are directly connected to the FPGA for minimum data latency. In the standard logic, the A/Ds have an interface component that receives the data, provides digital error correction, and a FIFO memory for buffering.

The two DAC channels have are 16-bit and have a maximum update rate of 500MSPS in dual channel mode, or 1 GSPS in single channel mode. The DAC also has optional interpolation modes of 2x and 4x. The DAC can also operate without any interpolation. Coarse mixing functions permit the DAC to move the output to several Nyquist zones.

Data flows between the IO and the host or system using a packet system
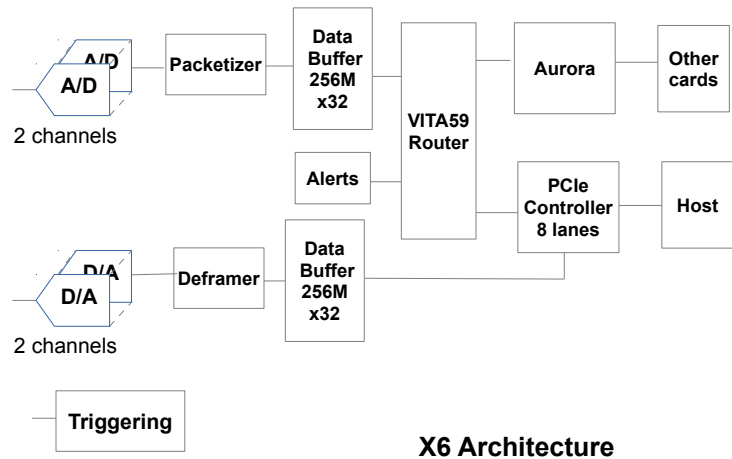
X6 Architecture

The A/D and DAC channels operate synchronously for simultaneously sampling systems using the external clock input. Controls for triggering allow precise control over the collection of data and are integrated into the FPGA logic. Trigger modes include frames of programmable size, pulse repetition interval, external and software. Multiple cards can sample simultaneously by using external trigger inputs. The trigger component in the logic can be customized in the logic to accommodate a variety of triggering requirements.

A non-volatile ROM is used to store the calibration coefficients for the analog and is programmed during factory test.

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FPGA Core

The X6 Module family has a Virtex6 FPGA and memory at its core for DSP and control. The Virtex6 FPGA is capable of over 1 Tera MACs (SX315T operating at 500 MHz internally) with over 1300 DSP elements in the SX315T FPGA. In addition to the raw processing power, the FPGA fabric integrates logic, memory and connectivity features that make the FPGA capable of applying this processing power to virtually any algorithm and sustaining performance in real-time. The FPGA has direct access to four banks of 1GB DRAM. These memories allow the FPGA working space for computation, required by DSP functions like FFTs, and bulk data storage needed for system data buffering and algorithms like Doppler delay. A multiple-queue controller component in the FPGA implements multiple data buffers in the DRAM that is used for system data buffering and algorithm support.

The X6 module family uses the Virtex6 FPGA as a system-on-chip to integrate all the features for highest performance. As such, all IO, memory and host interfaces connect directly to the FPGA – providing direct connection to the data and control for maximum flexibility and performance. Firmware for the FPGA completely defines the data flow, signal processing, controls and host interfaces, allowing complete customization of the X6 module functionality. Logic utilization is typically <10% of the device.

PCI Express Host Interface

The X6 architecture delivers over 2 GB/s sustained data rates over PCI Express Gen2 using the Velocia packet system. The Velocia packet system is an application interface layer on top of the fundamental PCI Express interface that provides an efficient and flexible host interface supporting high data rates with minimal host support. Using the Velocia packet system, data is transferred to the host as variable sized packets using the PCIe controller interface. The packet data system controls the flow of packets to the host, or other recipient, using a credit system managed in cooperation with the host software. The packets may be transmitted continuously for streams of data from the A/Ds, or as occasional packets for status, controls and analysis results. For all types of applications, the data buffering and flow control system delivers high throughput with low latency and complete flexibility for data types and packet sizes to match the application requirements. Firmware components for assembling and dissembling packets are provided in the FrameWork Logic that allow applications to rapidly integrate data streams and controls into the packet system with minimum effort.

The PCI Express interface is implemented in the Virtex6 FPGA using 8 GTX serial ports, for a maximum bit rate of over 40 Gbps, full duplex. Data encoding and protocol limit practical in-system data rates to about 400 MB/s per lane. Since PCI Express is not a shared bus but rather a point-to-point channel, system architectures can achieve high sustained data rates between devices – resulting in higher system-level performance and lower overall cost.

System Data Plane Ports and Digital IO

The X6 module family has eight high speed serial data links on J16 for system interconnect, operating at up to 5 Gbps per link, full duplex. These links enable the X6 modules to integrate into switched fabric systems such as VPX to create powerful computing and signal processing architectures. The standard logic uses these lanes as two Aurora ports of 4 lanes each. Other protocols such as SRIO and SFPDP may be implemented in the FPGA.

J4 connector has 32 digital lines that connect to the FPGA. These digital IO lines are direct connections to the FPGA.

Module Management

The X6 family has temperature monitoring for the FPGA die to detect overheating. The temperature sensor is set so that power shuts when a critical temperature is exceeded. This function is independent of the FPGA.

The data acquisition process can be monitored using the module alert mechanism. The alerts provide information on the timing of important events such as triggering, overranges and thermal overload. Packets containing data about the alert including an absolute system timestamp of the alert, and other information such as current temperature. This provides a precise overview of the card data acquisition process by recording the occurrence of these real-time events making the card

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easier to integrate into larger systems.

FPGA Configuration

The modules uses a FLASH memory for the Virtex 6 FPGA image. This FLASH can be programmed in-system using a software applet. There are two images in the FLASH: an application image and a "golden" image as a backup.

During development, the JTAG interface to the FPGA is used for development tools such as ChipScope and MATLAB. The FPGA JTAG connector is compatible with Xilinx Platform USB Cable.

Software Tools

Software development tools for the module provides comprehensive support including device drivers, data buffering, card controls, and utilities that allow developers to be productive from the start. At the most fundamental level, the software tools deliver data buffers to your application without the burden of low-level real-time control of the cards. Software classes provide C++ developers a powerful, high-level interface to the card that makes real-time, high speed data acquisition easier to integrate into applications.

Software for data logging and analysis are provided with every module. Data can be logged to system memory at full rate or to disk drives at rates supported by the drive and controller. Triggering and sample rate controls allow you to use the module's performance in your applications without ever writing code. Innovative software applets include *Binview* which provides data viewing, analysis and import to MATLAB for large data files.

Support for the Microsoft, Embarcadero and GNU C++ toolchains is provided. Supported OSes include Windows, Linux and VxWorks. For more information, the software tools User Guide and on-line help may be downloaded.

Logic Tools

High speed DSP, analysis, customized triggering and other unique features may be added to the module by modifying the logic. The FrameWork Logic tools provide support for RTL and MATLAB developments. The standard logic provides a hardware interface layer that allows designers to concentrate on the application-specific portions of the design. Designer can build upon the Innovative components for packet handling, hardware interfaces and system functions, the Xilinx IP core library, and third party IP. RTL source for the FrameWork Logic is provided for customization for most components. Each design is provided as a Xilinx ISE project, with a ModelSim testbench illustrating logic functionality.
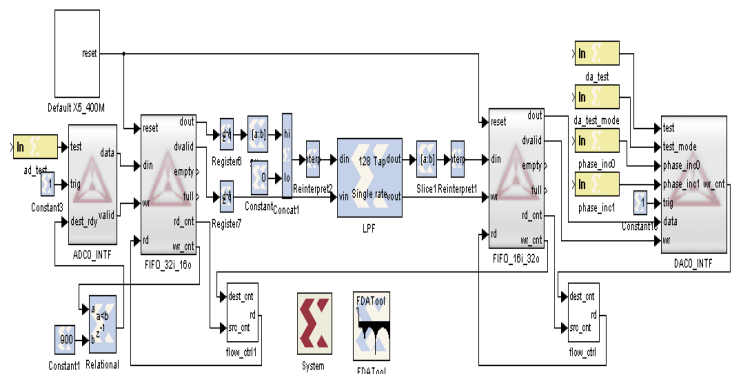
Using MATLAB Simulink for Logic Design

The MATLAB Board Support Package (BSP) allows logic development using Simulink and Xilinx System Generator. These tools provide a graphical design environment that integrates the logic into MATLAB Simulink for complete hardware-in-the-loop testing and development. This is an extremely power design methodology, since MATLAB can be used to generate, analyze and display the signals in the logic real-time in the system. Once the development is complete, the logic can be embedded in the FrameWork logic using the RTL tools.

The FrameWork Logic User sales brochure and User Guide more fully detail the development tools. Some of the more important logic functions are shown here.

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Logic Core	Description	Features
PCIe Interface	Interface to PCI Express bus supporting x1 to x8 lanes, Gen1 or Gen2. Implements Velocia packet system and Wishbone SOC bus.	Supports sustained data rates of up to 2 GB/s. Automates DMA transfers to the system using Velocia packet protocol. Wishbone SOC bus provides flexible bus architecture for designers.
Aurora Interface	Interface to x4 Aurora port for system expansion and data communicaitons.	Provides up to 1 GB/s data port to other cards for system expansion and data plane integration. Sub-channel support for messaging.
Router	Velocia packet router.	Dynamically steers packets amongst source and destination logic components.
Packetizer	Creates Velocia or VITA 49 packets.	Data packetizing and buffering for logic components for integration into Velocia packet system.
Deframer	Parses Velocia packets and dissembles them.	Deframer is used to extract data payloads from packets for logic component integration into Velocia packet system.

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Digital Transceiver

Digital Transceiver is a turnkey solution providing integrated data logging, playback, digital down-conversion (DDC), digital up-conversion (DUC), spectrum analyzer (FFT) in the compact system. The solution consists of three parts: the FPGA-based analog digitizer module, an eInstrument PC, and the firmware/software package to capture and analyze the data immediately.

A development kit is available to support creation of advanced custom firmware by logic developers. Netlist versions of the IP cores used to build the Digital Transceiver are provided, so developers can integrate with their own custom cores to create an enhanced transceiver design.

Product	DDC	DUC	FFT
V605	2 channels; bandwidth: 2 KHz – 43 MHz	2 channels; bandwidth: 2 KHz – 43 MHz	1ch, 32K

Table 1. Digital transceiver

Part Number	Target Module	Product	Description
55202-1	X6-400M	DDC, DUC and Spectrum Analysis	Framework Logic - 2 channels of IP-DDC-500MSPS, 2 channels of IP-DUC-500MSPS, and 1 channel of IP-FFT32K for Virtex-6 SX475T2

Table 2. Development kits

Part Number	Target Module	Product	Description
55102-1	X6-400M	DDC, DUC and Spectrum Analysis	Package - 2 channels of IP-DDC-500MSPS, 2 channels of IP-DUC-500MSPS, and 1 channel of IP-FFT32K for Virtex-6 SX475T2

Table 3. Software/firmware package

X6-400M

Applications Information

Cables

The X6-400M module uses coaxial cable assemblies for the analog I/O. The mating cable should have an SMA male connector and 50 ohm characteristic impedance for best signal quality.
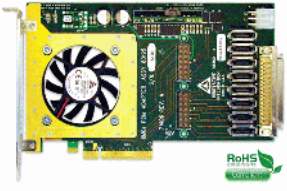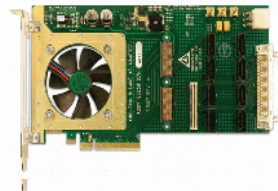
XMC Adapter Cards

XMC modules can be used in standard desktop, VPX or or compact PCI/PXI systems using a XMC adapter card. An auxiliary power connector to the PCI Express adapters provides additional power capability for XMC modules when the slot is unable to provide sufficient power. The adapter cards allow the XMC modules to be used in any PCIe or PCI system.

The X6 module family uses the auxiliary P16 connector as a private host interface. Eight Rocket IO lanes with digital IO signals provide support for data transfer rates up to 2.0 GB/s sustained, as well as sideband signals for control and status. Protocols such as Serial Rapid IO and Aurora may be implemented for host communications or custom protocols.

Note that the high speed Rocket IO lanes require a host card electrically capable of supporting the high speed signal pairs. Only the eight lane adapter, P/N 80173 is suitable for high speed P16 applications.

The VPX adapter supports 3U air-cooled or conduction-cooled applications. The adapter has steering for ports A-C and IPMI support. REDI covers for 2-level maintenance applications are also available.

PCIe-XMC Adapter (80172) x1 PCIe to XMC Clock and trigger inputs	**PCIe-XMC Adapter x8 lane (80173)** x8 PCIe to XMC P16 x8 RIO ports to SATA2 connectors DIO to MDR68	**PCIe-XMC Adapter x8 lane (80259)** x8 PCIe to XMC P16 x8 RIO ports to SATA connectors DIO to MDR68 Preferred for X6 Modules	**PCI-XMC Adapter (80167)** 64-bit, 133 MHz PCI-X host x4 PCIe to XMC
VPX-XMC Adapter (80262-6) 3U conduction-cooled VPX adapter Configurable port A-D mapping Optional REDI covers	**Compact PCI-XMC Adapter (80207)** 64-bit, 133 MHz PCI-X host x4 PCIe to XMC PXI triggers and clock support		

X6-400M

Applications that need remote or portable IO can use either the eInstrument PC or eInstrument Node with X6 modules. The VPXI system supports multiple card systems with integrated timing and data plane features.

eInstrument PC with Dual PCI Express XMC Modules (90199 or 90201)	**eInstrument DAQ Node – Remote IO using cabled PCI Express (90181)**
Windows/Linux embedded PC	PCI Express system expansion
Intel Core2Duo or low power Atom available	Up to 7 meter cable
8x USB, GbE, cable PCIe, VGA	electrically isolated from host computer
High speed x8 interconnect between modules	software transparent
GPS disciplined, programmable sample clocks and triggers to XMCs	Supports standalone operation for X6 modules
100 MB/s, 400 GB datalogger	
9-18VDC operation	
3U VPX PC with Four Expansion Slots and Integrated Timing (90271)	
3U VPX, air-cooled chassis with backplane	
Runs Windows, Linux, VxWorks	
Intel Dual Core i5 or i7, 8GB, 256MB SSD	
4x USB, GbE, x8 cable PCIe, Displayport, T	
Integrated timing clocks and triggers with GPS option	
400 MB/s, 1TB datalogger	
AC or DC operation	

X6-400M

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