XA-SDF

INTERCONNECT SYSTEMS
a molex company

PCI Express XMC Module with Four (4) 24-bit, 2.5 MSPS Sigma-Delta ADCs and Artix-7 FPGA

V0.5

FEATURES

- 4x 24-bit, 2.5 MSPS Sigma-Delta A/D channels
- Input range ± 5V (Differential)
- 4.1 kΩ / 2.54kΩ Input Impedance (Differential / Single-Ended)
- 100 dB typ. Dynamic Range (2.5 MHz Output Data Rate)
- 100 dB typ. SNR (2.5 MHz Output Data Rate)
- -103 dB typ. THD (2.5 MHz Output Data Rate)
- Guaranteed monotonic to 24 bits; 0.00076% typ. INL
- Lowpass FIR filter with default or programmable coefficients
- DIO on P16 (18 differential pairs)
- Xilinx Artix-7 FPGA
- DDR3 Memory
- Precision on-board programmable or external reference clock
- Synchronized system sampling using common reference clock and triggers
- Front Panel External Reference and Trigger Inputs
- Framed, software or external triggering
- Log acquisition timing and events
- Power management features
- PCI Express 2.0 XMC Module (75x150 mm)
- Use in any PCI Express desktop, compact PCI/PXI, PXIe, or cabled PCI Express application

APPLICATIONS

- Industrial Automation and Controls
- Multichannel Data Acquisition Systems
- Scientific and Industrial equipment
- Test and Measurement

SOFTWARE

- Data Acquisition, Logging and Analysis applications provided
- Windows/Linux Drivers
- C++ Host Tools
- VHDL Logic Tools

XILINX

The XA-SDF is an XMC IO module featuring four 24-bit, sigma-delta ADCs capable of operating at output data rates of up to 2.5 MSPS. Timing is generated using an on-board PLL (LMK04806).

Flexible trigger methods include counted frames, software triggering and external triggering. The sample rate clock is either an external clock or on-board programmable precision clock source.

Data acquisition control, signal processing, buffering, and system interface functions are implemented in a Xilinx Artix-7 FPGA device. Two 256Mb x16 DDR3 type memories provide data buffering and FPGA computing memory.

The logic can be fully customized using VHDL and the FrameWork Logic toolset.

The PCI Express 2.0 interface supports data rates up to 1600 MB/s for unbuffered continuous data or burst data streams. When using a standard configuration involving DDR3 buffered data, a continuous data rate up to 1300 MB/s is supported.

18 Differential (LVDS) Digital IO (DIO) Pairs along with 4 pairs of RX/TX high-speed Serial Link lanes are available on the XMC P16 connector.

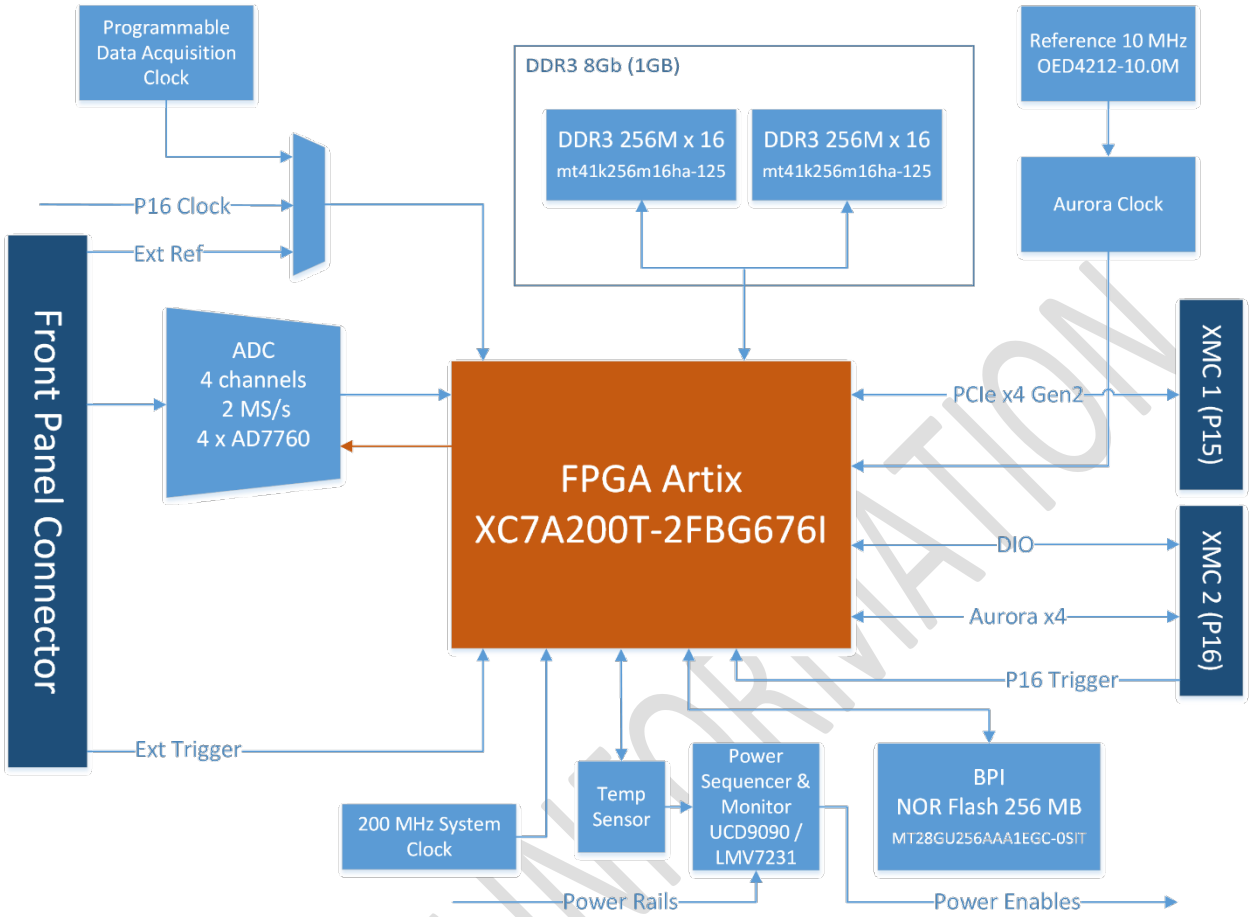

Fig. 1 XA-SDF Block Diagram

This electronics assembly can be damaged by ESD. Interconnect Systems International, LLC recommends that all electronic assemblies and components circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

Product	Part Number	Description
XA-SDF	80431-0-L0	XA-SDF XMC Module (w/ Heatsink) and Cable
	80431-1-L0	XA-SDF XMC Module (no Heatsink) and Cable
	80431-2-L0	XA-SDF XMC Module (no Heatsink) with Cable and Breakout Board
	80431-3-L0	XA-SDF XMC Module (w/ Heatsink) with Cable and Breakout Board
Logic		
XA-SDF FrameWork Logic	55303-1	FRAMEWORK LOGIC SUPPORT FOR XA-SDF
Cables		
SMA to BNC cable	67048G	SMA to BNC cable
Adapters		
XMC-PCIe x8 Adapter	80363-2-L0	XMC-PCIe x8 Adapter Card – XMC Standard – Internal Power
XMC-PCIe x8 Adapter	80363-3-L0	XMC-PCIe x8 Adapter Card – XMC Standard – External Power
Embedded PC Hosts		
SBC-Nano	90654-0-L0	SBC-NANO x4 PCIE 1 Gbe DEV KIT XA/X6
	90660-0-L0	SBC-NANO x4 PCIE 1 Gbe DEV KIT XA X6 GPS
	90662-0-L0	SBC-NANO x4 PCIE 1 Gbe DEV KIT XA X6 IEEE
	90664-0-L0	SBC-NANO XA_X6 WITH GPS UTILITY
SBC-DUO	90602-0-L0	EPC-DUO SE LMK04828 NO TIMING MODULE
	90602-0-L0	EPC-DUO SE LMK04828 GPS-500 CMOS
	90602-0-L0	EPC-DUO SE LMK04828 GPS LC_XO
	90602-0-L0	EPC-DUO SE LMK04828 GPS-500 LVDS
	90602-0-L0	EPC-DUO SE LMK04828 IEEE-1588
	90602-0-L0	EPC-DUO DIFF LMK04828 NO TIMING MODULE
	90602-0-L0	EPC-DUO DIFF LMK04828 GPS-500 CMOS
	90602-0-L0	EPC-DUO DIFF LMK04828 GPS LC_XO
	90602-0-L0	EPC-DUO DIFF LMK04828 GPS-500 LVDS
	90602-0-L0	EPC-DUO DIFF LMK04828 IEEE-1588
	90602-0-L0	EPC-DUO SE LMK048281NO TIMING MODULE
	90602-0-L0	EPC-DUO SE LMK04821 GPS-500 CMOS
	90602-0-L0	EPC-DUO SE LMK04821 GPS LC_XO
	90602-0-L0	EPC-DUO SE LMK048281GPS-500 LVDS

	90602-0-L0	EPC-DUO SE LMK048281 IEEE-1588
	90602-0-L0	EPC-DUO DIFF LMK04821 NO TIMING MODULE
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	90602-0-L0	EPC-DUO DIFF LMK04821 GPS-500 LVDS
	90602-0-L0	EPC-DUO DIFF LMK04821 IEEE-1588

XA-SDF

Standard Features

General	
Inputs	4
Connector	Samtec ERF8-013-01-L-D-RA-L-TR
Input Range	-5V < Vin < 5V (Differential)
Input Impedance	4.1 kΩ (typ) driven differentially 2.54 kΩ (typ) driven single-ended
ADC Device	AD7760
ADC Update Rate	Up to 2.5 MSPS using a 40 MHz serial clock.
Oversampling rate	Programmable (8x through 256x)
Filtering	A combination of up to three (3) FIR decimation filters, one of which is programmable.
Calibration	Factory calibrated. Gain error is digitally corrected and stored in non-volatile calibration coefficients memory.

Host Interface	
Type	PCI Express Gen 2
Sustained Data Rate	Up to 6 GB/sec*
Connector	XMC P15

Note: PCIe max speed and the sustained data rate are dependent on the system where the XA-SDF module is deployed and cannot be guaranteed by ISI.

Clocks and triggering	
Clock Sources	System Reference: Onboard TCXO or External (Front Panel or P16) Master PLL: LMK04806
Front Panel External Clock Input	50 Ohm AC-coupled input
Jitter	<350 fs rms typ.
Triggering	Software or External (Front Panel or P16)
Front Panel Trigger Input	500 Ohm DC-coupled input

System Monitoring	
Alerts	Trigger, Queue Overflow, Channel Over-range, Timestamp Rollover, Temperature Warning, Temperature Failure, PLL Unlocked

FPGA	
Device	Xilinx Artix-7 Ultrascale XC7A200T-2FBG676I
Speed Grade	-2
Temperature Range	0°C to +100°C (Extended)
System Logic Cells	215,360
CLB Flip-Flops	269,200
Slices	33,650
Maximum Distributed RAM (Kb)	2,888
Total Block RAM (Kb)	13,140
GTP Transceivers	8
Configuration	QSPI flash memory or JTAG

Memories	
DRAM Size	8 Gb (1 GB) total; 2 devices @ 32Mb x 16 x 8 each
DRAM Type	SDRAM DDR3L (1.25 ns)

Digital IO Connector	
DIO pins, total	36 onboard
Signal Standards	LVCMOS18 default; see Xilinx select IO user guide (UG571). DIOs routed as differential pairs on P16 rows C and F (except C19 and F19 which can source 1.8V up to 500mA) to user circuits
Connector	XMC P16

Power Management	
Temperature Monitor	Accessible by the host software
Alarms	Software programmable warning and failure levels
Over-temperature Monitor	Failure level alarm disables power
Power Control	Power sequencing; power good indication
Heat Sinking	Conduction cooling (VITA20 subset) and optional fan support

Physicals	
Form Factor	Single width IEEE 1386 Mezzanine Card
Size	75 x 150 mm
Weight	~160g (w/o heatsink)
Hazardous Materials	Lead-free and RoHS compliant

ABSOLUTE MAXIMUM RATINGS				
Exposure to conditions exceeding these ratings may cause board damage!				
Parameter	**Min**	**Max**	**Units**	**Conditions**
Supply Voltage, 3.3V to GND	0	3.6	V	
Supply Voltage, VPWR to GND	0	14.0	V	
Operating Temperature	0	+70	℃	Non-condensing, forced air cooling required
Storage Temperature	-40	+100	℃	
ESD Rating	-	2,000	V	Human Body Model
Vibration	-	5	g	9-200 Hz, Class 3.3 per ETSI EN 300 019-1-3 V2.1.2 (2003-04)
Shock	-	40	g peak	Class 3.3 per ETSI EN 300 019-1-3 V2.1.2 (2003-04)

RECOMMENDED OPERATING CONDITIONS				
Parameter	**Min**	**Typ**	**Max**	**Units**
Supply Voltage, 3.3V	3.15	3.3	3.45	V
Supply Voltage, VPWR*	4.75	12.0	14.0	V
Operating Temperature	0		60	℃
Forced Air Cooling				Approximate 200 LFM

Note: XA-SDF is specified and tested with VPWR = 12.0 V.