XA-Servo

INTERCONNECT SYSTEMS
a molex company

PCI Express XMC Module with 16x 18-bit, 500 kSPS ADCs, 16x 16-bit, 2.5 MSPS DACs and Artix-7 FPGA

V0.5

FEATURES

- 16x 18-bit simultaneously sampling 500 kSPS A/D channels
- Two programmable Input Ranges (+/-5V and +/-10V) with Remote Ground Sensing
- 1 MΩ Input Impedance
- Overvoltage Input Clamp With 9-kV ESD
- DNL: ±0.5 LSB typ.; INL: ±2.0 LSB typ.
- SNR: 94 dB typ.; THD: −109 dB typ.
- On-Chip Digital Filter for Oversampling (OS)
- 24 kHz typ. 3 dB Bandwidth (±10-V Input, no OS)
- 16x 16-bit up to 2.5 MSPS D/A channels with 6 software programmable Output Ranges:
  Unipolar: 0V to 5V, 0V to 10V
  Bipolar: ±2.5V, ±5V, ±10V, –2.5V to 7.5V
- 4µs Settling Time to ±1 LSB
- +/-10 mA min Load Current
- Output Short Current protection
- 50 Ω Output Impedance
- DIO on P16 (19 differential pairs)
- Xilinx Artix-7 FPGA
- DDR3 Memory
- Precision on-board programmable or external reference clock
- Synchronized system sampling using common reference clock and triggers
- 1 PPS and Sync Inputs
- Framed, software or external triggering
- Log acquisition timing and events
- Power management features
- PCI Express 2.0 XMC Module (75x150 mm)
- Use in any PCI Express desktop, compact PCI/PXI, PXIe, or cabled PCI Express application

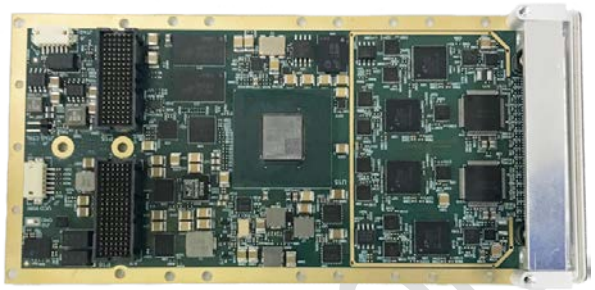
APPLICATIONS

- Industrial Automation and Controls
- Multichannel Data Acquisition Systems
- Scientific and Industrial equipment
- Test and Measurement

SOFTWARE

- Data Acquisition, Logging and Analysis applications provided
- Windows/Linux Drivers
- C++ Host Tools
- VHDL Logic Tools

XILINX



The XA-Servo is an XMC IO module featuring sixteen 18-bit, up to 500kSPS high-precision SAR A/D channels with high input impedance and remote ground sensing and sixteen 16-bit up to 2.5MSPS D/A channels with 4µs settling time, +/-10mA guaranteed output current designed for industrial, scientific, control, test and measurement applications.

Flexible trigger methods include counted frames, software triggering and external triggering. The sample rate clock is either an external clock or on-board programmable precision clock source.

Data acquisition control, signal processing, buffering, and system interface functions are implemented in a Xilinx Artix-7 FPGA device. Two 256Mb x16 DDR3 type memories provide data buffering and FPGA computing memory.

The logic can be fully customized using VHDL and the FrameWork Logic toolset.

The PCI Express 2.0 interface supports data rates up to 1600 MB/s for unbuffered continuous data or burst data streams. When using a standard configuration involving DDR3 buffered data, a continuous data rate up to 1300 MB/s is supported.

19 Differential (LVDS) Digital IO (DIO) Pairs along with 4 pairs of RX/TX high-speed Serial Link lanes are available on the XMC P16 connector.

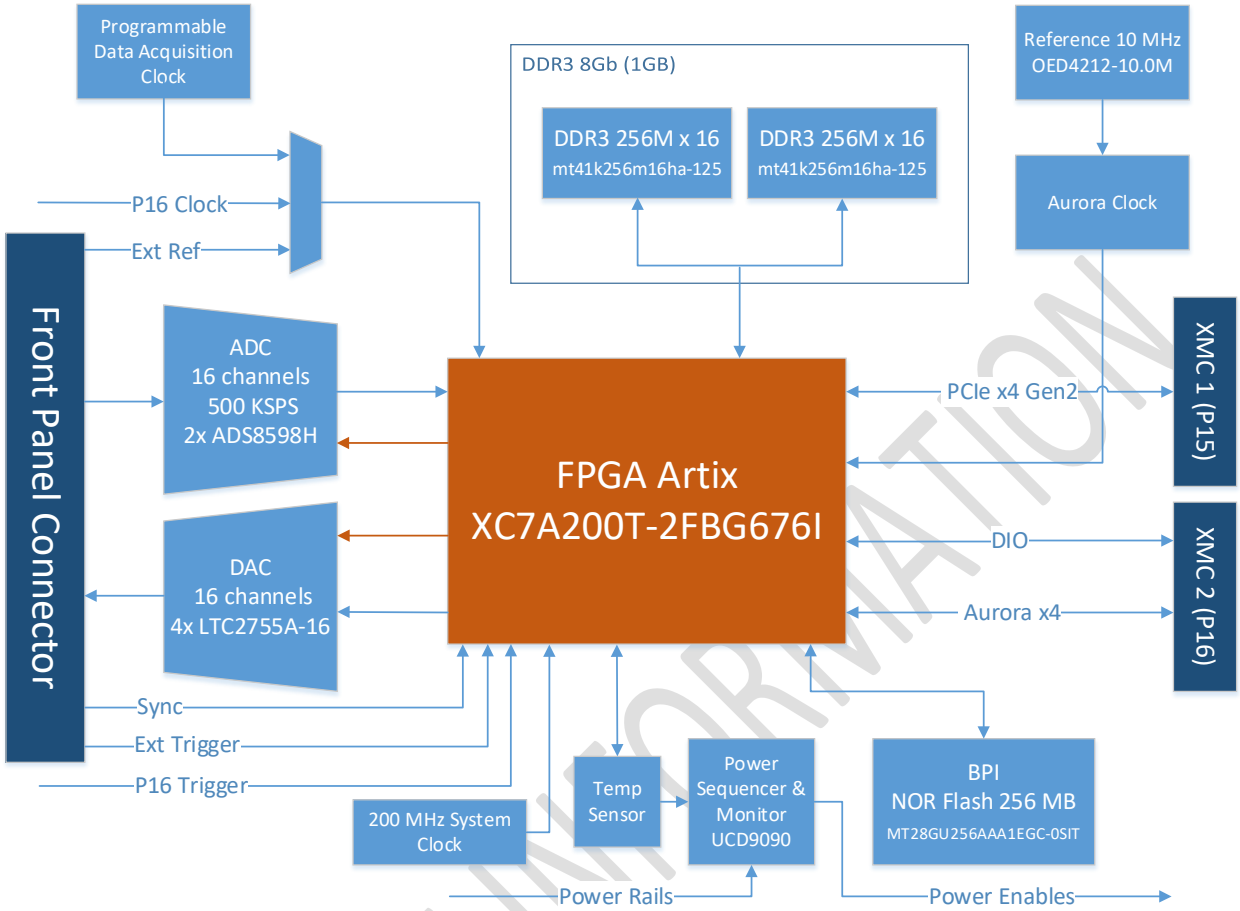


Fig. 1 XA-Servo Block Diagram