FMC-Servo

FMC Module with eight 16-bit, 500 kSPS A/D channels; eight 16-bit D/A channels with on-board timing controls.

V1.6

FEATURES

- Eight A/D Input Channels
  - 500 kSPS, 16-bit A/D
  - Differential, Gain Programmable
- Eight D/A Output Channels
  - 0.5µs Settling Time, 16-bit D/A
  - ± 10V Output Range
- Sample clocks and timing and controls
  - 10 MHz, ±250 ppb stability on-board reference.
  - Programmable PLL
  - Programmable Clock Frequency as low as 3.05 kHz
  - Integrated with FMC triggers
- FMC module, VITA 57.1
  - High Pin Count no SERDES required
  - Compatible with 2.5V VADJ
  - Power monitor and controls
- 12 W typical
- Conduction Cooling per VITA 20 subset
- Environmental ratings for -40 to 85C

  9g RMS sine, 0.1g^2/Hz random vibration

APPLICATIONS

- Industrial Instrumentation Systems
- Real-Time Control Systems
- Sensor Data Recording and Playback
- Machine Learning Systems

DESCRIPTION

The FMC-SERVO module features eight simultaneously sampling A/D and DACs, for use with an FPGA computing core. Low latency SAR A/D and fast-settling DACs support real-time servo control applications. The programmable input range and high input interface may connect directly to many sensors, while the output is capable of driving many transducers. Front panel digital IO can also be used as PWM or process controls.

Clock and trigger controls include support for consistent servo loop timing, counted frames, software triggering and external triggering. The sample rate clock is either an external clock or on-board programmable PLL clock source

The FMC-Servo power consumption is 12 W for typical operation. The module may be conduction cooled using VITA20 standard and a heat spreading plate. Ruggedization levels for wide-temperature operation from -40 to +85C operation and 0.1 g^2/Hz vibration. Conformal coating is available.

Support logic in VHDL is available for integration with FPGA carrier cards. Contact ISISales@Molex.com. Specific support for Innovative carrier cards includes integration with Framework Logic tools that support VHDL developers.

Software tools for Innovative carrier cards include host development C++ libraries and drivers for Windows and Linux, 64-bit. Application examples demonstrating the module features are provided.

* Sampling rates in an application depend on carrier and system design

FMC-Servo

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This electronics assembly can be damaged by ESD. Interconnect Systems International, LLC recommends that all electronic assemblies and components circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

Product	Part Number	Description
FMC-Servo	80339-0-L0 80339-1-L0 80339-2-L0	FMC-SERVO DIFFERENTIAL INPUTS/OUTPUTS FMC-SERVO SINGLE ENDED INPUTS/OUTPUTS FMC-SERVO DIFFERENTIAL INPUTS/OUTPUTS, INTERPOSER EXTENSION
Carrier Cards	80382-0-L0 80382-1-L0	PEX7-COP K325T -2 SPEED IND. TEMP. PEX7-COP K410T -2 SPEED IND. TEMP.
Embedded PCs	90502-3-L0 90502-4-0-L0	EPC-K7 INSTRUMENT WITH K325T2 FPGA EPC-K7 INSTRUMENT WITH K410T2 FPGA
Cables & Breakouts	80350-1-L0	FMC BREAKOUT ALL SMA WITH CABLE (Note 1)

Note 1. Options without SMA and Cable are available.

BLOCK DIAGRAM

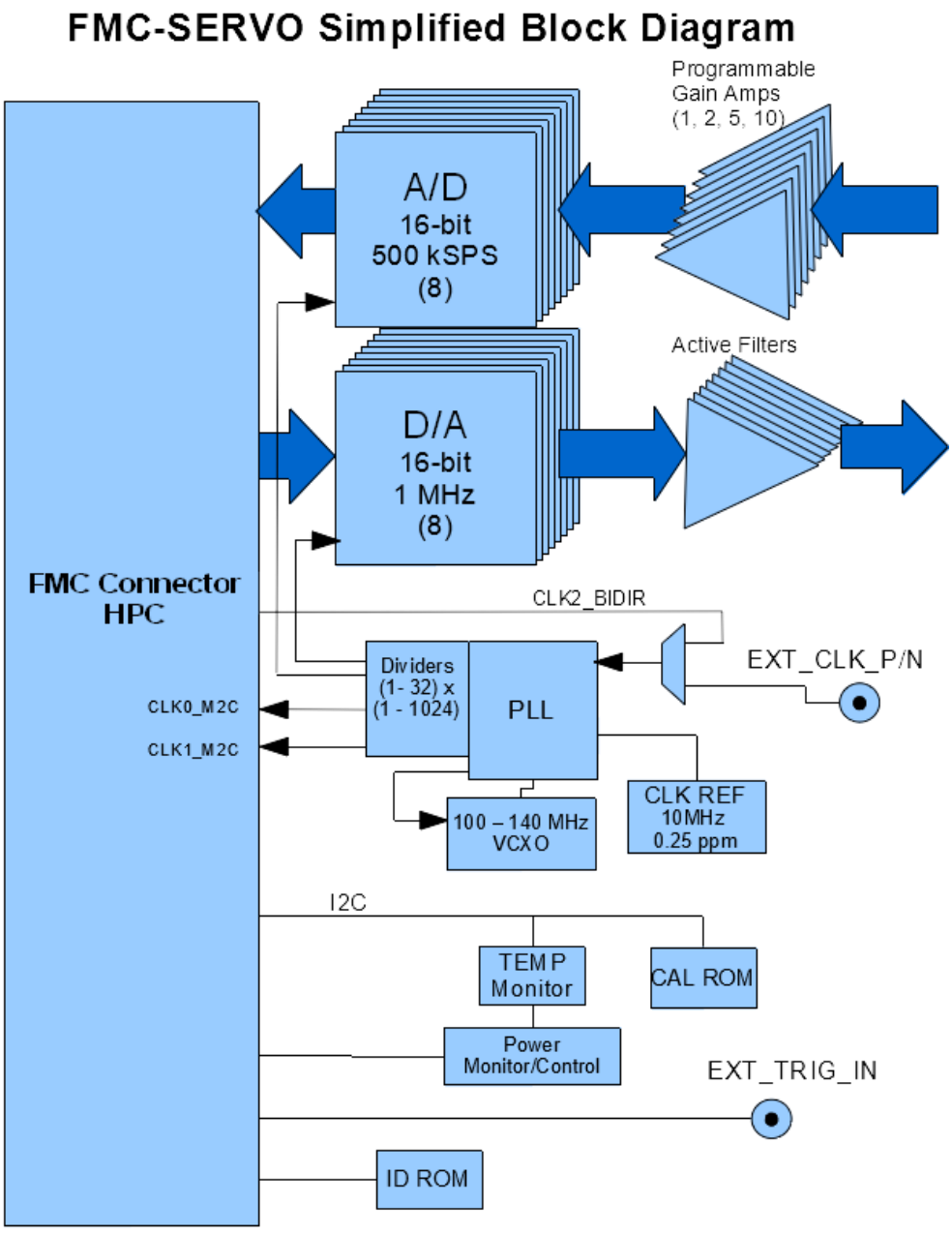


Figure 1. FMC-Servo Block Diagram

FMC-Servo

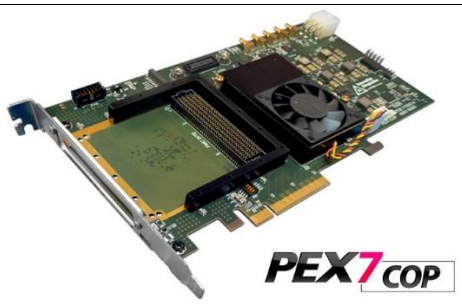


Figure 4. PEX7-COP Carrier board with Kintex 7 FPGA

Figure 5. ePC-K7, Windows/Linux Embedded Computer with Kintex-7 FPGA, Dual FMC IO Sites, Integrated Timing Support

Standard Features

Analog Inputs	
Inputs	8
Input Range	+/- 10V (Gain x1)
Input Type	Single Ended, DC Coupled
Size	Supports 84 x 55 mm modules (mini size)
Nominal Input Impedance	> 1 MΩ (DC, all versions). Dynamic impedance = 50 ohms (-1 config.) Dynamic impedance = 100 ohms (-0 config.) (pole = 165 ns)
A/D Device	Texas Instruments ADS8568 (500 KSPS, 16-bit)
Resolution	16-bit
ADC Sample Rate	<= 500 kSPS
Input Bandwidth	250 kHz (-3dB, est.) (DC-Coupled)
Analog Outputs	
Outputs	8
Output Range	±10V DC-coupled into high impedance load.
Output Type	Single ended, AC or DC coupled
Output Impedance	100 ohms (back terminated to guard against overshoot/undershoot)
DAC Device	Burr-Brown (TI) DAC8822 (x 4)
DAC Resolution	16-bit
DAC Update Rate	<= 1 MHz
FMC Interface	
IO	LA[33:0] pairs, HA[22:0] pairs, HB[12:0] pairs

Clocks and Triggering	
Clock Sources	External, or Internal, based on Analog Devices AD9510 followed by AD9508. Est. Jitter < 350 fs RMS VCXO: 100 – 140 MHz
PLL Reference	External or 10 MHz on-card 10 MHz ref is ±250 ppb -40 to +85C
PLL Resolution	> 12 kHz using 10 MHz reference Assumes PLL's "B" divider is configured with 8,191 divider ratio. May require adjustment of on-board PLL filter and parameters. This resolution is divided by the AD9510 / AD9508 divisors to calculate resolution at clock output. See "PLL Notes" below for additional information.
Phase Noise	-155 dBc / Hz @ 100 kHz offset (measured at reference frequency – phase noise at output will depend on PLL gain and output divisors.)
Triggering	External, software, acquire N frame Decimation 1:1 to 1:4095 in FPGA Channel Clocking All channels are synchronous Multi-card Synchronization External triggering input is used to synchronize sample clocks or an external clock and trigger may be used.
Physicals	

FMC-Servo

IO Standards	LA: LVDS HA: LVDS HB : LVCMOS 1.7V to 3.3V
Required Voltages	3.3V, 12V VADJ = 1.7 to 3.3 V
FMC Power	
Total	12.68 W (15W incl. full external Vadj load).
3.3V	< 20 mA (66 mW)
12V	1002 mA (12.02 W)
2.5V Adj	< 1.2A (2.64 W)
Heat Sinking	Conduction cooling supported, system level thermal design may be required

Form Factor	FMC VITA 57.1 single-width
Size	76.5 x 69 mm 10 mm mounting height
Weight	180g (approximate, contact factory if critical to application)
Hazardous Materials	Lead-free and RoHS compliant

Operating Environment Ratings

The FMC-Servo can be used in a variety of applications with different operating environment temperature, shock and vibration levels. Contact Sales for available Ruggedization Levels.

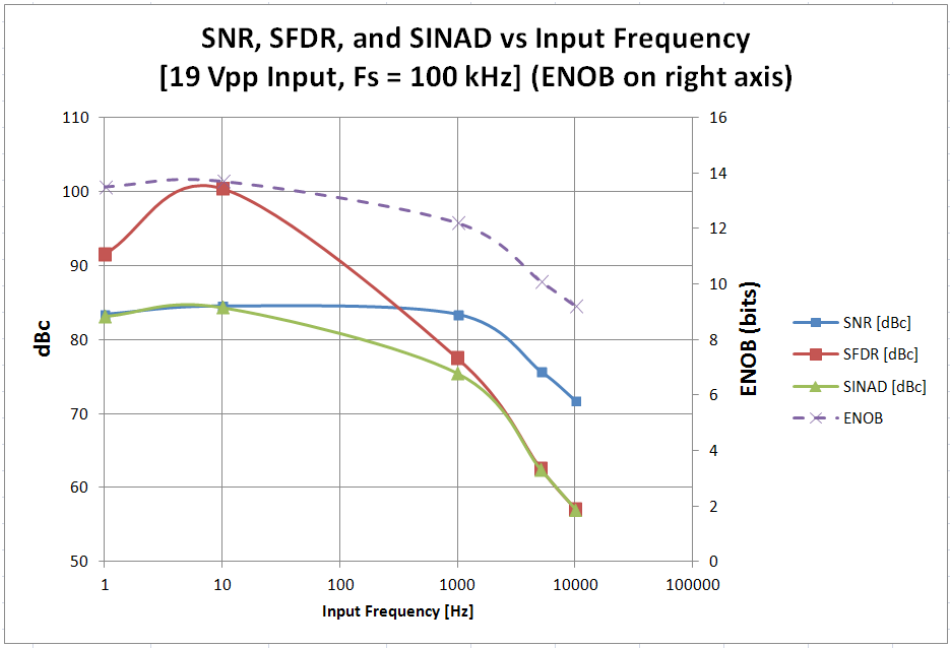
Environment Rating <ER>		**L0**	**L1**	**L2**	**L3**	**L4**
Environment		Office, controlled lab	Outdoor, stationary	Industrial	Vehicles	Military and heavy industry
Applications		Lab instruments, research	Outdoor monitoring and controls	Industrial applications with moderate vibration	Manned vehicles	Unmanned vehicles, missiles, oil and gas exploration
Cooling		Forced Air 2 CFM	Forced Air 2 CFM	Conduction	Conduction	Conduction
Operating Temperature		0 to +50C	-40 to +85C	-20 to +65C	-40 to +70C	-40 to +85C
Storage Temperature		-20 to +90C	-40 to +100C	-40 to +100C	-40 to +100C	-50 to +100C
Vibration	Sine	-	-	2g 20-500 Hz	5g 20-2000 Hz	10g 20-2000 Hz
	Random	-	-	0.04 g^2/Hz 20-2000 Hz	0.1 g^2/Hz 20-2000 Hz	0.1 g^2/Hz 20-2000 Hz
Shock		-	-	20g, 11 ms	30g, 11 ms	40g, 11 ms
Humidity		0 to 95%, non-condensing	0 to 100%	0 to 100%	0 to 100%	0 to 100%
Conformal coating			Conformal coating	Conformal coating, extended temperature range devices	Conformal coating, extended temperature range devices, Thermal conduction assembly	Conformal coating, extended temperature range devices, Thermal conduction assembly, Epoxy bonding for devices
Testing		Functional, Temperature cycling	Functional, Temperature cycling, Wide temperature testing	Functional, Temperature cycling, Wide temperature testing Vibration, Shock	Functional, Temperature cycling, Wide temperature testing Vibration, Shock	Functional, Testing per MIL-STD-810G for vibration, shock, temperature, humidity

ELECTRICAL CHARACTERISTICS

A/D ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range at 0°C to +60°C, unless otherwise noted.

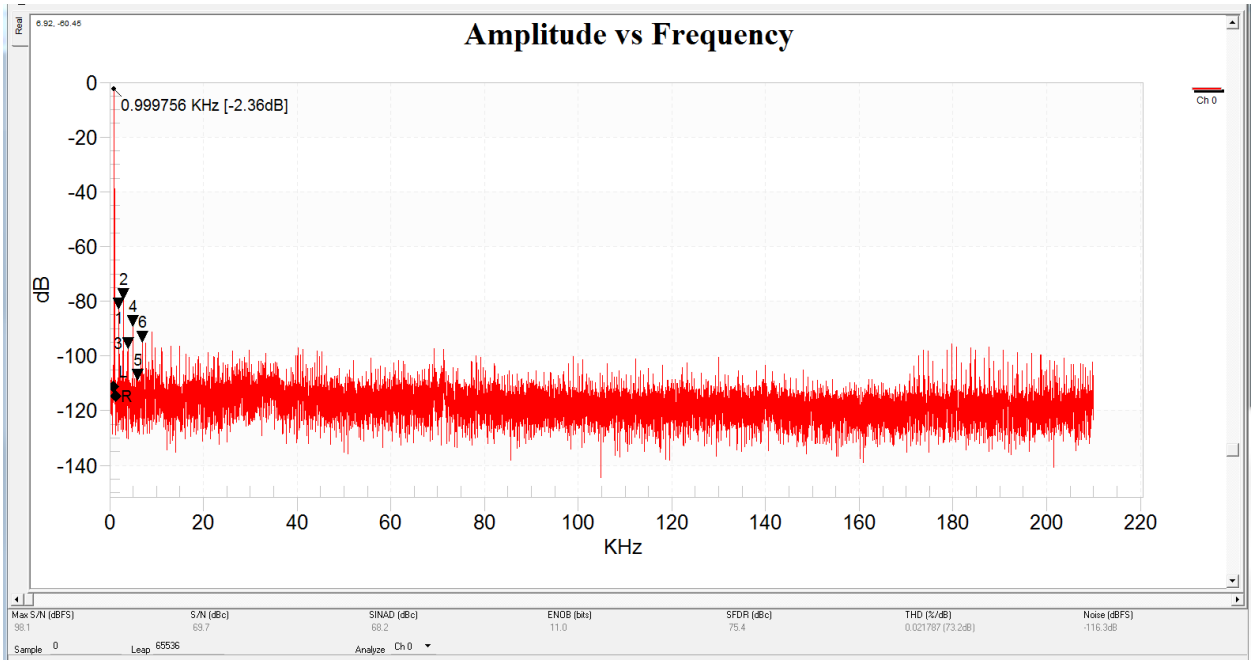
Parameter		Typ	Units	Notes
A/D Channels (typical)				
Static (DC input) INL		within ±2	LSBs	Based on deviation from linear regression straight-line fit to data
Bandwidth		200	kHz	-3dB, DC coupled inputs (includes input filtering)
Range	DC Coupled	+/-10	V	Absolute maximum from ground, gain setting = 1
SNR		83.4	dB	Fin = 1 kHz, 100 kSPS
THD		-75.9	dBc	Fin = 1 kHz, 100 kSPS
SFDR		77.5	dB	Fin = 1 kHz, 100 kSPS
Offset Error (absolute value maximum)		1	mV	After factory calibration: average of 64K samples after warm-up.
Gain Error (absolute value maximum)		0.5	%	After factory calibration: gain setting =1, after warm-up.



D/A ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range at 0°C to +60°C, unless otherwise noted.

Parameter	Typ	Units	Notes
DAC Channels (Typical)			
Analog Output Range	+/- 10	V	Typical, DC Coupled
Static (DC output) INL	within ±2	LSBs	Based on deviation from linear regression straight-line fit to data
Analog Output Bandwidth	400	kHz	including response of output active filter excluding sample-and-hold effect (sinc roll-off)
SFDR	75.4	dBc	Fout = 1 kHz, Fs = 420 kHz, 20 Vpp (DAC to ADC end-to-end)
SNR	69.7	dBc	Fout = 1 kHz, Fs = 420 kHz, 20 Vpp (DAC to ADC end-to-end)
THD	-73.2	dBc	Fout = 1 kHz, Fs = 420 kHz, 20 Vpp (DAC to ADC end-to-end)
Channel Crosstalk	<-64	dB	Aggressor = 200 kHz, adjacent channel.
Noise floor	-121.3	dBFS/ Hz	Fout = 1 kHz, Fs = 420 kHz, 20 Vpp (based on 64K FFT, DAC to ADC end-to-end)
Gain Error	<0.5	% of FS	After factory calibration (and after warm-up)
Offset Error	<10	mV	After factory calibration (and after warm-up)



Notes

Gain Definition

FMC-Servo is specified and tested with a low source impedance (ideal voltage source or 50 ohm source impedance, both negligible compared to the input impedance of the board). The FMC-Servo nominal gain is calibrated at the 1X or 0dB setting, resulting in a full-scale output. The internal hardware (raw) gain of the FMC-Servo may be different, such as when the particular board being calibrated comes in at a gain slightly lower than unity and the ADC output is digitally corrected to achieve overall accuracy.

Digital Calibration Note

The FMC-Servo can be digitally calibrated for offset and gain. However if the signal is clipped (outside the A/D range) the information is lost, so the raw gain is typically designed for a signal level at the A/D that is slightly less than A/D Full Scale in the bandwidth of interest to allow the nominal input range to be measured accurately without clipping when digitally calibrated.

PLL Notes

The output clock is produced by an integer division (1~32)*(1~1,024) of the VCXO output. The VCXO has a tuning range of 100 – 140 MHz. This tuning range limits the range of frequencies that can be produced by integer division. For output clock frequencies below 46.67 MHz (140 MHz / 3) some combination of VCXO frequency and division ratio can be chosen to produce any arbitrary output clock frequency because the various divider output frequency ranges overlap. For example, if the AD9510 divisor is chosen to be 32 and the AD9508 divisor is chosen to be 1024, the tuning range is 3051.758 kHz – 4272.461 kHz. The next highest range (31 x 1024) is 3150.202 kHz – 4410.282 kHz which overlaps the lower range. Table 1 shows one possible programming scheme that ensures continuous coverage between an output frequency of 3.05 kHz and 46.67 MHz.

Beyond the ability to successfully synthesize a prescribed output clock frequency as outlined above, the tuning resolution limits the ability to realize the corresponding VCO output frequency exactly. The architecture of the loop requires that the VCO frequency be a rational fraction multiple (i.e., a quotient of integers) of the input reference frequency (in this case, 10 MHz). Two issues limit the achievable resolution: (1) the precision of the rational fraction necessary to produce the necessary VCO frequency and (2) the value of the feedback divide ratio (the numerator of the rational fraction) required to produce that VCO frequency since it affects the stability parameters of the PLL. The required divide ratios are not always obvious – for example, a number of VCXO frequencies (within the tuning range) are available to produce a 501 kHz output: 100.2 MHz (501 kHz x 200), 100.7 MHz, (501 kHz x 202), etc. through 139.779 MHz (501 kHz x 279).

Of the above options, the best possible choice of VCXO frequency would be one in which the numerator and denominator of the rational fraction are the smallest possible numbers. From this standpoint 100.7 MHz (10 MHz x (501/50)) is preferable to 139.779 MHz (10 MHz x (2530/181)). With such a wide tuning range (± 16.6 %) there a number of choices available which would produce the same output frequency. Also, which particular VCXO frequencies would result in the lowest possible divisors is not always obvious – 125.25 MHz (501 kHz x 250) results in even smaller divisors (10 MHz x (238/19)) than does 100.7 MHz.

AD9508 Div	AD9510 Div	Fmin	Fmax
1024	3 - 32	3.05 kHz	45.57 kHz
96	3 - 32	45.57 kHz	486.11 kHz
9	3 - 32	486.11 kHz	5.185 MHz
1	3 - 32	5.185 MHz	46.667 MHz

Table 1. Range of output clock frequencies showing continuous coverage in the tuning range.

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FMC Connector Pin Assignments

P1 Pins	P1 Pin Name	FMC-Servo Net
A1	GND	GND
A2	DP1_M2C_P	N/C
A3	DP1_M2C_N	N/C
A4	GND	GND
A5	GND	GND
A6	DP2_M2C_P	N/C
A7	DP2_M2C_N	N/C
A8	GND	GND
A9	GND	GND
A10	DP3_M2C_P	N/C
A11	DP3_M2C_N	N/C
A12	GND	GND
A13	GND	GND
A14	DP4_M2C_P	N/C
A15	DP4_M2C_N	N/C
A16	GND	GND
A17	GND	GND
A18	DP5_M2C_P	N/C
A19	DP5_M2C_N	N/C
A20	GND	GND
A21	GND	GND
A22	DP1_C2M_P	N/C
A23	DP1_C2M_N	N/C
A24	GND	GND
A25	GND	GND
A26	DP2_C2M_P	N/C
A27	DP2_C2M_N	N/C
A28	GND	GND
A29	GND	GND
A30	DP3_C2M_P	N/C
A31	DP3_C2M_N	N/C
A32	GND	GND
A33	GND	GND
A34	DP4_C2M_P	N/C
A35	DP4_C2M_N	N/C
A36	GND	GND
A37	GND	GND
A38	DP5_C2M_P	N/C
A39	DP5_C2M_N	N/C
A40	GND	GND

B1	CLK_DIR	3P3V
B2	GND	GND
B3	GND	GND
B4	DP9_M2C_P	N/C
B5	DP9_M2C_N	N/C
B6	GND	GND
B7	GND	GND
B8	DP8_M2C_P	N/C
B9	DP8_M2C_N	N/C
B10	GND	GND
B11	GND	GND
B12	DP7_M2C_P	N/C
B13	DP7_M2C_N	N/C
B14	GND	GND
B15	GND	GND
B16	DP6_M2C_P	N/C
B17	DP6_M2C_N	N/C
B18	GND	GND
B19	GND	GND
B20	GBTCLK1_M2C_P	N/C
B21	GBTCLK1_M2C_N	N/C
B22	GND	GND
B23	GND	GND
B24	DP9_C2M_P	N/C
B25	DP9_C2M_N	N/C
B26	GND	GND
B27	GND	GND
B28	DP8_C2M_P	N/C
B29	DP8_C2M_N	N/C
B30	GND	GND
B31	GND	GND
B32	DP7_C2M_P	N/C
B33	DP7_C2M_N	N/C
B34	GND	GND
B35	GND	GND
B36	DP6_C2M_P	N/C
B37	DP6_C2M_N	N/C
B38	GND	GND
B39	GND	GND
B40	RE50	N/C

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C1	GND	GND
C2	DP0_C2M_P	N/C
C3	DP0_C2M_N	N/C
C4	GND	GND
C5	GND	GND
C6	DP0_M2C_P	N/C
C7	DP0_M2C_N	N/C
C8	GND	GND
C9	GND	GND
C10	LA06_P	ADC_D0
C11	LA06_N	ADC_D1
C12	GND	GND
C13	GND	GND
C14	LA10_P	ADC_D2
C15	LA10_N	ADC_D3
C16	GND	GND
C17	GND	GND
C18	LA14_P	ADC_D4
C19	LA14_N	ADC_D5
C20	GND	GND
C21	GND	GND
C22	LA18_P_CC	ADC_D6
C23	LA18_N_CC	ADC_D7
C24	GND	GND
C25	GND	GND
C26	LA27_P	FMC_ADC_CS_N
C27	LA27_N	FMC_ADC_RD_N
C28	GND	GND
C29	GND	GND
C30	SCL	FMC_SCL
C31	SDA	FMC_SDA
C32	GND	GND
C33	GND	GND
C34	GA0	FMC_G0
C35	12P0V	12P0V
C36	GND	GND
C37	12P0V	12P0V
C38	GND	GND
C39	3P3V	3P3V
C40	GND	GND

D1	PG_C2M	FMC_PG_C2M
D2	GND	GND
D3	GND	GND
D4	GBTCLK0_M2C_P	N/C
D5	GBTCLK0_M2C_N	N/C
D6	GND	GND
D7	GND	GND
D8	LA01_P_CC	ADC_D8
D9	LA01_N_CC	ADC_D9
D10	GND	GND
D11	LA05_P	ADC_D10
D12	LA05_N	ADC_D11
D13	GND	GND
D14	LA09_P	ADC_D12
D15	LA09_N	ADC_D13
D16	GND	GND
D17	LA13_P	ADC_D14
D18	LA13_N	ADC_D15
D19	GND	GND
D20	LA17_P_CC	FMC_ADC_STBY_N
D21	LA17_N_CC	FMC_ADC_RESET
D22	GND	GND
D23	LA23_P	REF_SEL
D24	LA23_N	FMC_ADC_BUSY
D25	GND	GND
D26	LA26_P	FMC_ADC_GAIN_D0
D27	LA26_N	FMC_ADC_GAIN_D1
D28	GND	GND
D29	TCK	N/C
D30	TDI	N/C
D31	TDO	N/C
D32	3P3VAUX	3P3V_AUX
D33	TMS	N/C
D34	TRST_L	N/C
D35	GA1	FMC_G1
D36	3P3V	3P3V
D37	GND	GND
D38	3P3V	3P3V
D39	GND	GND
D40	3P3V	3P3V

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E1	GND	GND
E2	HA01_P_CC	N/C
E3	HA01_N_CC	N/C
E4	GND	GND
E5	GND	GND
E6	HA05_P	N/C
E7	HA05_N	N/C
E8	GND	GND
E9	HA09_P	N/C
E10	HA09_N	N/C
E11	GND	GND
E12	HA13_P	N/C
E13	HA13_N	N/C
E14	GND	GND
E15	HA16_P	N/C
E16	HA16_N	N/C
E17	GND	GND
E18	HA20_P	N/C
E19	HA20_N	N/C
E20	GND	GND
E21	HB03_P	N/C
E22	HB03_N	N/C
E23	GND	GND
E24	HB05_P	N/C
E25	HB05_N	N/C
E26	GND	GND
E27	HB09_P	N/C
E28	HB09_N	N/C
E29	GND	GND
E30	HB13_P	N/C
E31	HB13_N	N/C
E32	GND	GND
E33	HB19_P	N/C
E34	HB19_N	N/C
E35	GND	GND
E36	HB21_P	N/C
E37	HB21_N	N/C
E38	GND	GND
E39	VADJ	VADJ
E40	GND	GND

F1	PG_M2C	PG_M2C
F2	GND	GND
F3	GND	GND
F4	HA00_P_CC	N/C
F5	HA00_N_CC	N/C
F6	GND	GND
F7	HA04_P	N/C
F8	HA04_N	N/C
F9	GND	GND
F10	HA08_P	N/C
F11	HA08_N	N/C
F12	GND	GND
F13	HA12_P	N/C
F14	HA12_N	N/C
F15	GND	GND
F16	HA15_P	N/C
F17	HA15_N	N/C
F18	GND	GND
F19	HA19_P	N/C
F20	HA19_N	N/C
F21	GND	GND
F22	HB02_P	N/C
F23	HB02_N	N/C
F24	GND	GND
F25	HB04_P	N/C
F26	HB04_N	N/C
F27	GND	GND
F28	HB08_P	N/C
F29	HB08_N	N/C
F30	GND	GND
F31	HB12_P	N/C
F32	HB12_N	N/C
F33	GND	GND
F34	HB16_P	N/C
F35	HB16_N	N/C
F36	GND	GND
F37	HB20_P	N/C
F38	HB20_N	N/C
F39	GND	GND
F40	VADJ	VADJ

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G1	GND	GND
G2	CLK1_M2C_P	CLK1_M2C_P
G3	CLK1_M2C_N	CLK1_M2C_N
G4	GND	GND
G5	GND	GND
G6	LA00_P_CC	DAC_D0
G7	LA00_N_CC	DAC_D1
G8	GND	GND
G9	LA03_P	DAC_D2
G10	LA03_N	DAC_D3
G11	GND	GND
G12	LA08_P	DAC_D4
G13	LA08_N	DAC_D5
G14	GND	GND
G15	LA12_P	DAC_D6
G16	LA12_N	DAC_D7
G17	GND	GND
G18	LA16_P	DAC_A0
G19	LA16_N	DAC_A1
G20	GND	GND
G21	LA20_P	FMC_DAC_LDAC
G22	LA20_N	DAC_RST_N
G23	GND	GND
G24	LA22_P	DAC_WR0
G25	LA22_N	DAC_WR1
G26	GND	GND
G27	LA25_P	DAC_WR2
G28	LA25_N	DAC_WR3
G29	GND	GND
G30	LA29_P	FMC_PLL_SDIO
G31	LA29_N	FMC_PLL2_CS_N
G32	GND	GND
G33	LA31_P	FMC_PLL_STATUS1
G34	LA31_N	FMC_PLL_SYNC1
G35	GND	GND
G36	LA33_P	N/C
G37	LA33_N	FMC_PLL_SYNC2
G38	GND	GND
G39	VADJ	VADJ
G40	GND	GND

H1	VREF_A_M2C	N/C
H2	PRSNT_M2C_L	GND
H3	GND	GND
H4	CLK0_M2C_P	CLK0_M2C_P
H5	CLK0_M2C_N	CLK0_M2C_N
H6	GND	GND
H7	LA02_P	DAC_D8
H8	LA02_N	DAC_D9
H9	GND	GND
H10	LA04_P	DAC_D10
H11	LA04_N	DAC_D11
H12	GND	GND
H13	LA07_P	DAC_D12
H14	LA07_N	DAC_D13
H15	GND	GND
H16	LA11_P	DAC_D14
H17	LA11_N	DAC_D15
H18	GND	GND
H19	LA15_P	ADC_GAIN_CH0
H20	LA15_N	ADC_GAIN_CH1
H21	GND	GND
H22	LA19_P	ADC_GAIN_CH2
H23	LA19_N	ADC_GAIN_WR
H24	GND	GND
H25	LA21_P	ADC_SLEEP
H26	LA21_N	DAC_CLK_SEL
H27	GND	GND
H28	LA24_P	FMC_PLL1_CS_N
H29	LA24_N	FMC_PLL_SCLK
H30	GND	GND
H31	LA28_P	FMC_TRIGOUT_P
H32	LA28_N	FMC_TRIGOUT_N
H33	GND	GND
H34	LA30_P	TRIG_SEL
H35	LA30_N	EXT_CLK_SEL
H36	GND	GND
H37	LA32_P	N/C
H38	LA32_N	FMC_TEMP_ALERT
H39	GND	GND
H40	VADJ	VADJ

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J1	GND	GND
J2	CLK3_BIDIR_P	CLK3_BIDIR_P
J3	CLK3_BIDIR_N	CLK3_BIDIR_N
J4	GND	GND
J5	GND	GND
J6	HA03_P	N/C
J7	HA03_N	N/C
J8	GND	GND
J9	HA07_P	N/C
J10	HA07_N	N/C
J11	GND	GND
J12	HA11_P	N/C
J13	HA11_N	N/C
J14	GND	GND
J15	HA14_P	N/C
J16	HA14_N	N/C
J17	GND	GND
J18	HA18_P	N/C
J19	HA18_N	N/C
J20	GND	GND
J21	HA22_P	N/C
J22	HA22_N	N/C
J23	GND	GND
J24	HB01_P	N/C
J25	HB01_N	N/C
J26	GND	GND
J27	HB07_P	N/C
J28	HB07_N	N/C
J29	GND	GND
J30	HB11_P	N/C
J31	HB11_N	N/C
J32	GND	GND
J33	HB15_P	N/C
J34	HB15_N	N/C
J35	GND	GND
J36	HB18_P	N/C
J37	HB18_N	N/C
J38	GND	GND
J39	VIO_B_M2C	N/C
J40	GND	GND

K1	VREF_B_M2C	N/C
K2	GND	GND
K3	GND	GND
K4	CLK2_BIDIR_P	CLK2_BIDIR_P
K5	CLK2_BIDIR_N	CLK2_BIDIR_N
K6	GND	GND
K7	HA02_P	N/C
K8	HA02_N	N/C
K9	GND	GND
K10	HA06_P	N/C
K11	HA06_N	N/C
K12	GND	GND
K13	HA10_P	N/C
K14	HA10_N	N/C
K15	GND	GND
K16	HA17_P_CC	N/C
K17	HA17_N_CC	N/C
K18	GND	GND
K19	HA21_P	N/C
K20	HA21_N	N/C
K21	GND	GND
K22	HA23_P	N/C
K23	HA23_N	N/C
K24	GND	GND
K25	HB00_P_CC	N/C
K26	HB00_N_CC	N/C
K27	GND	GND
K28	HB06_P_CC	N/C
K29	HB06_N_CC	N/C
K30	GND	GND
K31	HB10_P	N/C
K32	HB10_N	N/C
K33	GND	GND
K34	HB14_P	N/C
K35	HB14_N	N/C
K36	GND	GND
K37	HB17_P_CC	N/C
K38	HB17_N_CC	N/C
K39	GND	GND
K40	VIO_B_M2C	VADJ

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