PEX7-COP

V1.1

INTERCONNECT SYSTEMS
a molex company

PCI Express Desktop/Server Coprocessor with Kintex-7 FPGA Computing Core and FMC I/O Site

FEATURES

- Desktop/Server 3/4 full-length FPGA Coprocessor Card
- FMC HPC I/O site (VITA 57) with x8 10.0 Gbps MGT lanes, 80 LVDS pairs (LA, HA, HB full support)
- FPGA Computing Core
- Xilinx Kintex-7 K325T or K410T
- Single Bank 256Mb x 64 DDR3 (2048 MB total)
- 256Mb BPI Configuration FLASH
- External clock input
- External trigger input supports multi-card synchronization and coordinated sampling
- 1 PPS Input
- 8 lane PCIe Express Gen 2 interface providing 4 GB/s burst and 3.2 GB/s sustained transfer rates
- On-board USB to JTAG programmer allows FPGA programming without external hardware
- 14-pin JTAG header with Xilinx compatible pinout
- < 15W typical power excluding FMC
- Temperature and power monitoring

APPLICATIONS

- FPGA co-processing and acceleration
- Wireless Receivers – LTE, WiMAX, SATCOM
- RADAR, Signal Intelligence
- Medical Imaging
- High Speed Data Recording and Playback
- IP development

SOFTWARE

- VHDL FrameWork Logic
- Windows/Linux Drivers
- C++ DevKit

FMC XILINX®

DESCRIPTION

The PEX7-COP is a flexible FPGA co-processor card that integrates a Kintex-7 FPGA computing core with an industry-standard FMC I/O card on a three-quarter length PCI Express desktop or server card.

The FPGA computing core features the Xilinx Kintex-7 FPGA family and is offered in two densities, K325T or K410T. The K410T FPGA provides over 2000 DSP MAC elements operating at up to 500 MHz. The FPGA core has a 2048 MB DDR3 DRAM bank attached.

For system communications, the PEX7-COP utilizes a PCI Express 8 lane Gen 2 port capable of up to 3.2 GB/s sustained operation with 4 GB/s burst rate.

An FMC site, conforming to VITA 57 standard, provides configurable I/O for the PEX7-COP. The FMC site has full support for the high pin count connector (HPC), with 80 LVDS pairs and 8 high-speed lanes (TX/RX) at up to 10 Gbps per lane directly connected to the FPGA. The FMC site is readily adapted to application-specific custom cards.

The FPGA design can be fully customized using VHDL and the FrameWork Logic Devkit.

A software development kit for host development includes C++ libraries and 64-bit drivers for Windows and Linux. An application demonstrating the card's features is provided with supported FMC Cards.

PEX7-COP

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Interconnect Systems International, LLC standard warranty. Production processing does not necessarily include testing of all parameters.

This electronics assembly can be damaged by ESD. Interconnect Systems International, LLC recommends that all electronic assemblies and components circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

Product	Part Number	Description
PEX7-COP, K325T, -2 SPEED, IND. TEMP	80382-0-L0	PEX7-COP with XC7K325T-2FFG900I FPGA
PEX7-COP, K410T, -2 SPEED, IND. TEMP	80382-1-L0	PEX7-COP with XC7K410T-2FFG900I FPGA
Breakout Board with 36” Cable	80350-1-L0	DIO Breakout Board, all SMA Connectors with 3 ft EQCD Ribbon Coaxial Cable 67227
Breakout Board, no Cable	80350-5-L0	DIO Breakout Board, all SMA Connectors, 67227 Cable is not included
36” Cable Ribbon Coax Cable	67227	Cable Assembly, 3 ft EQCD Ribbon Coaxial Cable
PCIe Satellite DIO, PEX7-COP	80386-0-L0	Expansion DIO Board for PEX7-COP with 1 ft EQCD Ribbon Coaxial Cable 67246
Cable Assy, Ribbon Coax, 2x20	67246	1 ft EQCD Ribbon Coaxial Cable from PCIe Satellite DIO board to PEX7-COP
PEX7-COP FrameWork Logic	55212	PEX7-COP FrameWork Logic support package for RTL. Check with sales for specific FMC support and pricing.
Software	57003	II Installation Flash Memory Athena (USB Flash Drive)

PEX7-COP

BLOCK DIAGRAM

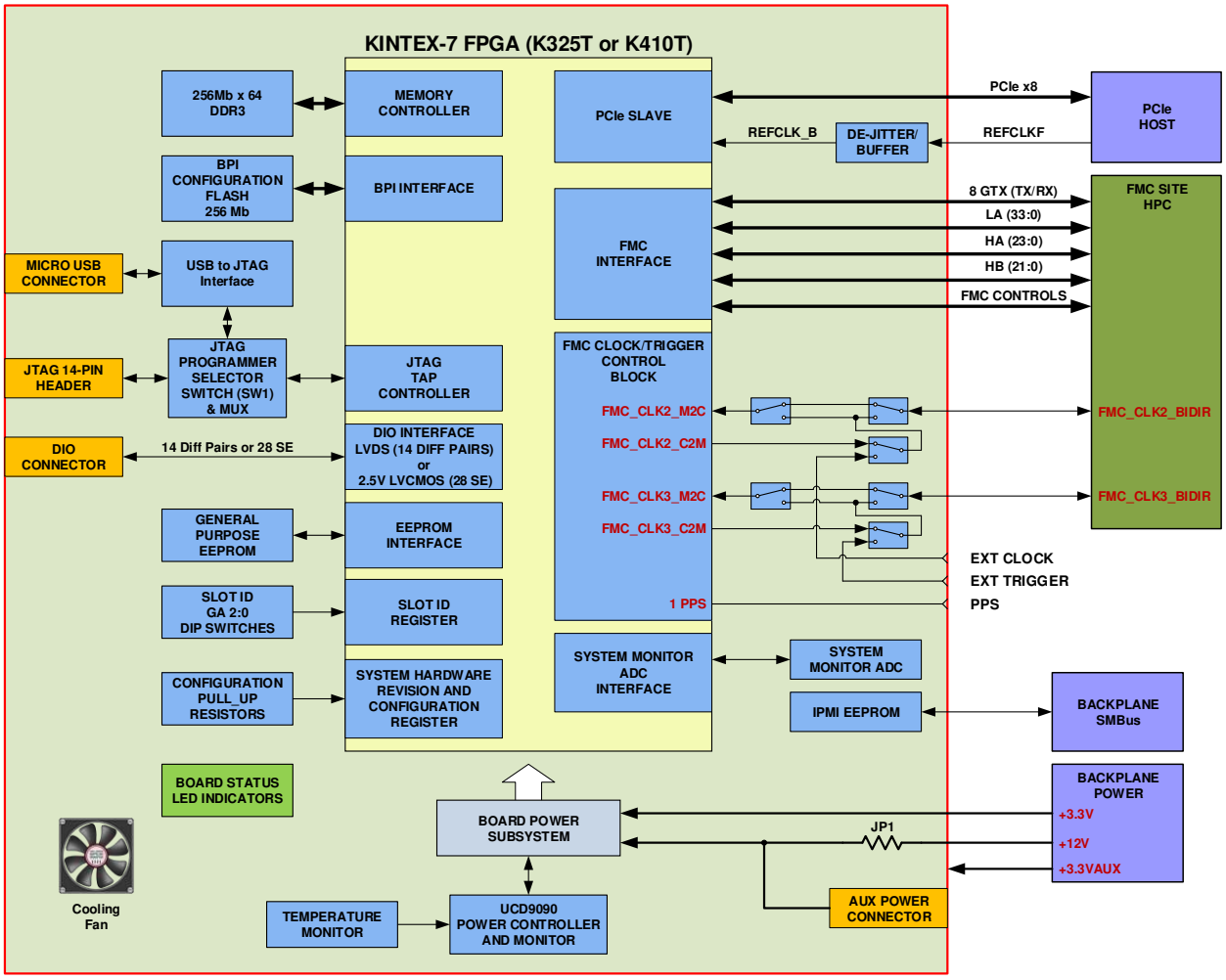


Figure 1. PEX7-COP Block Diagram

Operating Environment Ratings

The PEX7-COP is environmentally rated **L0** (Office or Controlled Laboratory use). Contact ISI sales if other environmental rating and/or ruggedization level is desired.

PEX7-COP

Standard Features

Physicals	
Form Factor	PCI Express, ~ 3/4 Full Size card
Size	206.4 mm x 111.1 mm (8.125 in x 4.375 in)
Weight	~213g (7.5 oz), without FMC
Hazardous Materials	Lead-free and RoHS compliant

Power (PEX7-COP only w/o FMC)	
3.3V (+/-5%)	1A Maximum. Supplied by the host computer
12V (+/-5%)	1.2A Maximum. Supplied by the host computer OR from the J8 Auxiliary Connector (jumper JP1 must be removed to avoid potential damage)
3.3VAUX (+/-5%)	50mA Maximum. Supplied by the host computer
Power Consumption	15W typical

FMC Power Available	
3.3V (+/-5%)	3A Maximum. Supplied by the host computer
12V (+/-5%)	2A Maximum. Supplied by the host computer OR from the J8 Auxiliary Connector (jumper JP1 must be removed to avoid potential damage)
Vadj (+/-5%; 2.5V standard)	4A Maximum. Generated on the PEX7-COP card
3.3VAUX (+/-5%)	20mA Maximum. Supplied by the host computer

Power and Thermal Control	
Temperature Monitor	Software with programmable alarms
Over-temperature Monitor	Disables power supplies
Alerts	Temperature Warning, Temperature Failure, Power Faults
Alert Timestamping	5 ns resolution, 32-bit counter
Power Control	LPDDR3 deep sleep mode FMC power controls
Heat Sinking	Heatsink with fan, on FPGA

FMC Site	
Specification	VITA 57 FMC, HPC (High Pin Count)
High Speed Pairs	8 lanes (Tx/Rx pair); 10 Gbps max rate
Signal Pairs	80 diff pairs total LA: 34 diff pairs (Kintex-7 FPGA) HA: 24 diff pairs (Kintex-7 FPGA) HB: 22 diff pairs (Kintex-7 FPGA)
I/O Standards	LA: all I/O standards available in an HR bank, with VCCO = VADJ voltage HA: all I/O standards available in an HR bank, with VCCO = VADJ voltage HB: all I/O standards available in an HR bank, with VCCO = VIO_B voltage Choice of I/O standards is also constrained by FPGA limitations on which standards can be used together in the same HR bank.

FPGA	
Device	Xilinx Kintex-7; K325T or K410T depending on option
Speed Grade	-2
Logic Cells	K325T: 326K K410T: 406K
Flip-Flops/Slices	K325T: 407K /50K K410T: 508K /63K
DSP48E1 elements / Total Block RAM	K325T: 840 / 16,020 Kb K410T: 1540 / 28,620 Kb
GTX Transceivers	16 available: 8 for PCIe, 8 for FMC High Speed Pairs Max 10.3125 Gb/s data rate is supported for speed grade -2
Configuration	JTAG or FLASH; In-system reprogrammable

Memories	
DDR3 SDRAM	256Mb x 64 (2048MB) Clock rate 800 MHz (DDR3 1600)
BPI Configuration FLASH	Parallel NOR FLASH Memory 256Mb, Eight 32Mb partitions
General Purpose EEPROM	SPI FLASH, 128Mb
IPMI EEPROM / Temperature sensor	8 Kb EEPROM

Host Interface	
PCI Express	x8 Lanes Gen2 Supports PCI Express Base 2.1 specification at Gen1 and Gen2 data rates

Sample Clocks and Triggering (SSMC Jacks)	
External Clock (connector J11 / CLK_P) *	Single-ended; AC-coupled; 0.3Vp-p min, 1.5Vp-p max; 50 Ohm Input Impedance
External Trigger (connector J13/ TRIG_P) *	Single-ended; DC-coupled; Vin low = 0V to 0.7V; Vin high = 1.7V to 2.5V; 500 Ohm Input Impedance
1 PPS (connector J5 / PPS)	Single ended; DC-Coupled; Vin low = 0V to 0.6V; Vin high = 1.2V to 5.5V; 10 KOhm Input Impedance

Note: Contact ISI sales for other external clock and trigger input configuration options, such as differential input signaling (LVDS), customized input impedance and coupling type.

Application DIO	
DIO Bits	28, arranged as 14 pairs
Signal Standards*	Single Ended: LVCMOS25 (2.5V) – **NOT 3.3V TOLERANT!** Differential Pairs: LVDS25

Note: Please refer to Xilinx document DS182 “Kintex-7 FPGAs Data Sheet: DC and AC Switching Characteristics” for details on DIO signaling requirements. **Exceeding Xilinx specified absolute maximum ratings may damage the Kintex-7 FPGA and render the PEX7-COP card non-operational!**

ABSOLUTE MAXIMUM RATINGS				
Exposure to conditions exceeding these ratings may cause card damage!				
Parameter	**Min**	**Max**	**Units**	**Conditions**
Supply Voltage, 3.3V to GND	0	3.6	V	
Supply Voltage, 12.0V to GND	0	14.0	V	
Operating Temperature	0	+70	℃	Non-condensing
Storage Temperature	-40	+100	℃	
ESD Rating	-	2,000	V	Human Body Model
Vibration	-	5	g	9-200 Hz, Class 3.3 per ETSI EN 300 019-1-3 V2.1.2 (2003-04)
Shock	-	40	g peak	Class 3.3 per ETSI EN 300 019-1-3 V2.1.2 (2003-04)

RECOMMENDED OPERATING CONDITIONS				
Parameter	**Min**	**Typ.**	**Max**	**Units**
Supply Voltage, 3.3V	3.15	3.3	3.45	V
Supply Voltage, 12.0V	11.4	12.0	12.6	V
Operating Temperature	10		60	℃
Forced Air Cooling		200		LFM

Architecture and Features

The PEX7-COP architecture integrates a Xilinx Kintex-7 FPGA computing core with an FMC module on a PCI Express desktop/server three-quarter length card. Communication with the host PC is provided by a x8 Gen2 PCI Express link. The architecture tightly couples the FPGA to the FMC and enables the module to perform real-time signal processing with low latency and extremely high rates. It is well-suited for FPGA co-processing and front-end signal processing applications in wireless, RADAR and medical imaging.

FMC Module Site

The PEX7-COP FMC site is a VITA 57 standard compliant HPC (High Pin Count) site for I/O or system expansion. The FMC module directly connects to the FPGA with 80 pairs of LVDS (160 single-ended) and 8 lanes of high-speed serial. The serial lanes connect to the FPGA MGT ports.

FMC modules are integrated with the PEX7-COP by application logic in the FPGA that provides interface control and data communications. The flexible and generic nature of the FMC interface allows specialized application logic to be conveniently designed for each FMC module type.

The FMC modules mount on the PEX7-COP conductive cooling rails which provide effective heat transfer path for the module.

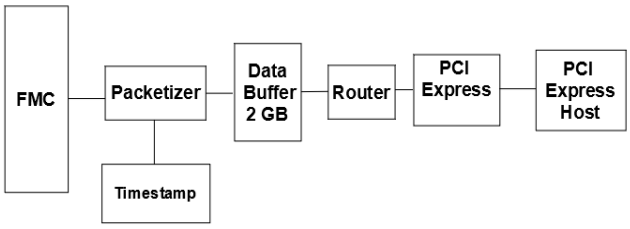


Figure 2. Typical PEX7-COP system architecture showing data packet flow between the IO and the host

Table below shows the FMC site signal connections on the PEX7-COP card.

Signal Name	J3 Pin	Kintex-7 Pin	Kintex 7 Bank /MGT Quad	Signal Name	J3 Pin	Kintex-7 Pin	Kintex 7 Bank/MGT Quad
FMC_HA_0_N	F5	C27	Bank 16	FMC_LA_0_N	G7	F13	Bank 18
FMC_HA_0_P	F4	D27	Bank 16	FMC_LA_0_P	G6	G13	Bank 18
FMC_HA_1_N	E3	C26	Bank 16	FMC_LA_1_N	D9	G14	Bank 18
FMC_HA_1_P	E2	D26	Bank 16	FMC_LA_1_P	D8	H14	Bank 18
FMC_HA_2_N	K8	B29	Bank 16	FMC_LA_2_N	H8	K16	Bank 18
FMC_HA_2_P	K7	C29	Bank 16	FMC_LA_2_P	H7	L16	Bank 18
FMC_HA_3_N	J7	H27	Bank 16	FMC_LA_3_N	G10	K15	Bank 18
FMC_HA_3_P	J6	H26	Bank 16	FMC_LA_3_P	G9	L15	Bank 18
FMC_HA_4_N	F8	G30	Bank 16	FMC_LA_4_N	H11	L13	Bank 18
FMC_HA_4_P	F7	H30	Bank 16	FMC_LA_4_P	H10	L12	Bank 18
FMC_HA_5_N	E7	A28	Bank 16	FMC_LA_5_N	D12	J13	Bank 18
FMC_HA_5_P	E6	B28	Bank 16	FMC_LA_5_P	D11	K13	Bank 18
FMC_HA_6_N	K11	E25	Bank 16	FMC_LA_6_N	C11	J14	Bank 18
FMC_HA_6_P	K10	F25	Bank 16	FMC_LA_6_P	C10	K14	Bank 18
FMC_HA_7_N	J10	A27	Bank 16	FMC_LA_7_N	H14	G15	Bank 18
FMC_HA_7_P	J9	B27	Bank 16	FMC_LA_7_P	H13	H15	Bank 18
FMC_HA_8_N	F11	D23	Bank 16	FMC_LA_8_N	G13	J12	Bank 18
FMC_HA_8_P	F10	E23	Bank 16	FMC_LA_8_P	G12	J11	Bank 18
FMC_HA_9_N	E10	D24	Bank 16	FMC_LA_9_N	D15	H16	Bank 18
FMC_HA_9_P	E9	E24	Bank 16	FMC_LA_9_P	D14	J16	Bank 18
FMC_HA_10_N	K14	B24	Bank 16	FMC_LA_10_N	C15	H12	Bank 18

FMC_HA_10_P	K13	C24	Bank 16	FMC_LA_10_P	C14	H11	Bank 18
FMC_HA_11_N	J13	A23	Bank 16	FMC_LA_11_N	H17	B12	Bank 18
FMC_HA_11_P	J12	B23	Bank 16	FMC_LA_11_P	H16	C12	Bank 18
FMC_HA_12_N	F14	C30	Bank 16	FMC_LA_12_N	G16	E11	Bank 18
FMC_HA_12_P	F13	D29	Bank 16	FMC_LA_12_P	G15	F11	Bank 18
FMC_HA_13_N	E13	E30	Bank 16	FMC_LA_13_N	D18	A12	Bank 18
FMC_HA_13_P	E12	E29	Bank 16	FMC_LA_13_P	D17	A11	Bank 18
FMC_HA_14_N	J16	A30	Bank 16	FMC_LA_14_N	C19	C11	Bank 18
FMC_HA_14_P	J15	B30	Bank 16	FMC_LA_14_P	C18	D11	Bank 18
FMC_HA_15_N	F17	F28	Bank 16	FMC_LA_15_N	H20	E15	Bank 18
FMC_HA_15_P	F16	G28	Bank 16	FMC_LA_15_P	H19	E14	Bank 18
FMC_HA_16_N	E16	F27	Bank 16	FMC_LA_16_N	G19	C14	Bank 18
FMC_HA_16_P	E15	G27	Bank 16	FMC_LA_16_P	G18	D14	Bank 18
FMC_HA_17_N	K17	B25	Bank 16	FMC_LA_17_N	D21	D13	Bank 18
FMC_HA_17_P	K16	C25	Bank 16	FMC_LA_17_P	D20	D12	Bank 18
FMC_HA_18_N	J19	E26	Bank 16	FMC_LA_18_N	C23	E13	Bank 18
FMC_HA_18_P	J18	F26	Bank 16	FMC_LA_18_P	C22	F12	Bank 18
FMC_HA_19_N	F20	D28	Bank 16	FMC_LA_19_N	H23	A13	Bank 18
FMC_HA_19_P	F19	E28	Bank 16	FMC_LA_19_P	H22	B13	Bank 18
FMC_HA_20_N	E19	A26	Bank 16	FMC_LA_20_N	G22	B15	Bank 18
FMC_HA_20_P	E18	A25	Bank 16	FMC_LA_20_P	G21	C15	Bank 18
FMC_HA_21_N	K20	F30	Bank 16	FMC_LA_21_N	H26	A15	Bank 18
FMC_HA_21_P	K19	G29	Bank 16	FMC_LA_21_P	H25	B14	Bank 18
FMC_HA_22_N	J22	F18	Bank 17	FMC_LA_22_N	G25	J18	Bank 17
FMC_HA_22_P	J21	G18	Bank 17	FMC_LA_22_P	G24	K18	Bank 17
FMC_HA_23_N	K23	B17	Bank 17	FMC_LA_23_N	D24	G20	Bank 17
FMC_HA_23_P	K22	C17	Bank 17	FMC_LA_23_P	D23	H20	Bank 17
FMC_HB_0_N	K26	AC27	Bank 13	FMC_LA_24_N	H29	H17	Bank 17
FMC_HB_0_P	K25	AB27	Bank 13	FMC_LA_24_P	H28	J17	Bank 17
FMC_HB_1_N	J25	AA26	Bank 13	FMC_LA_25_N	G28	H19	Bank 17
FMC_HB_1_P	J24	Y26	Bank 13	FMC_LA_25_P	G27	J19	Bank 17
FMC_HB_2_N	F23	W28	Bank 13	FMC_LA_26_N	D27	L18	Bank 17
FMC_HB_2_P	F22	W27	Bank 13	FMC_LA_26_P	D26	L17	Bank 17
FMC_HB_3_N	E22	AA28	Bank 13	FMC_LA_27_N	C27	H22	Bank 17
FMC_HB_3_P	E21	Y28	Bank 13	FMC_LA_27_P	C26	H21	Bank 17
FMC_HB_4_N	F26	Y29	Bank 13	FMC_LA_28_N	H32	C21	Bank 17
FMC_HB_4_P	F25	W29	Bank 13	FMC_LA_28_P	H31	D21	Bank 17
FMC_HB_5_N	E25	AB28	Bank 13	FMC_LA_29_N	G31	F22	Bank 17
FMC_HB_5_P	E24	AA27	Bank 13	FMC_LA_29_P	G30	G22	Bank 17
FMC_HB_6_N	K29	AD28	Bank 13	FMC_LA_30_N	H35	C22	Bank 17
FMC_HB_6_P	K28	AD27	Bank 13	FMC_LA_30_P	H34	D22	Bank 17
FMC_HB_7_N	J28	AC30	Bank 13	FMC_LA_31_N	G34	E21	Bank 17
FMC_HB_7_P	J27	AC29	Bank 13	FMC_LA_31_P	G33	F21	Bank 17
FMC_HB_8_N	F29	AA30	Bank 13	FMC_LA_32_N	H38	E20	Bank 17
FMC_HB_8_P	F28	Y30	Bank 13	FMC_LA_32_P	H37	F20	Bank 17
FMC_HB_9_N	E28	AE29	Bank 13	FMC_LA_33_N	G37	C16	Bank 17
FMC_HB_9_P	E27	AD29	Bank 13	FMC_LA_33_P	G36	D16	Bank 17
FMC_HB_10_N	K32	AB30	Bank 13	FMC_RX_0_N	C7	A7	Quad 118

FMC_HB_10_P	K31	AB29	Bank 13	FMC_RX_0_P	C6	A8	Quad 118
FMC_HB_11_N	J31	AF28	Bank 13	FMC_RX_1_N	A3	B5	Quad 118
FMC_HB_11_P	J30	AE28	Bank 13	FMC_RX_1_P	A2	B6	Quad 118
FMC_HB_12_N	F32	AK30	Bank 13	FMC_RX_2_N	A7	D5	Quad 118
FMC_HB_12_P	F31	AK29	Bank 13	FMC_RX_2_P	A6	D6	Quad 118
FMC_HB_13_N	E31	AF30	Bank 13	FMC_RX_3_N	A11	E3	Quad 118
FMC_HB_13_P	E30	AE30	Bank 13	FMC_RX_3_P	A10	E4	Quad 118
FMC_HB_14_N	K35	AJ29	Bank 13	FMC_RX_4_N	A15	F5	Quad 117
FMC_HB_14_P	K34	AJ28	Bank 13	FMC_RX_4_P	A14	F6	Quad 117
FMC_HB_15_N	J34	AH30	Bank 13	FMC_RX_5_N	A19	G3	Quad 117
FMC_HB_15_P	J33	AG30	Bank 13	FMC_RX_5_P	A18	G4	Quad 117
FMC_HB_16_N	F35	AK28	Bank 13	FMC_RX_6_N	B17	H5	Quad 117
FMC_HB_16_P	F34	AJ27	Bank 13	FMC_RX_6_P	B16	H6	Quad 117
FMC_HB_17_N	K38	AH29	Bank 13	FMC_RX_7_N	B13	K5	Quad 117
FMC_HB_17_P	K37	AG29	Bank 13	FMC_RX_7_P	B12	K6	Quad 117
FMC_HB_18_N	J37	AG28	Bank 13	FMC_TX_0_N	C3	A3	Quad 118
FMC_HB_18_P	J36	AG27	Bank 13	FMC_TX_0_P	C2	A4	Quad 118
FMC_HB_19_N	E34	AH27	Bank 13	FMC_TX_1_N	A23	B1	Quad 118
FMC_HB_19_P	E33	AH26	Bank 13	FMC_TX_1_P	A22	B2	Quad 118
FMC_HB_20_N	F38	AF27	Bank 13	FMC_TX_2_N	A27	C3	Quad 118
FMC_HB_20_P	F37	AF26	Bank 13	FMC_TX_2_P	A26	C4	Quad 118
FMC_HB_21_N	E37	AK26	Bank 13	FMC_TX_3_N	A31	D1	Quad 118
FMC_HB_21_P	E36	AJ26	Bank 13	FMC_TX_3_P	A30	D2	Quad 118
				FMC_TX_4_N	A35	F1	Quad 117
				FMC_TX_4_P	A34	F2	Quad 117
				FMC_TX_5_N	A39	H1	Quad 117
				FMC_TX_5_P	A38	H2	Quad 117
				FMC_TX_6_N	B37	J3	Quad 117
				FMC_TX_6_P	B36	J4	Quad 117
				FMC_TX_7_N	B33	K1	Quad 117
				FMC_TX_7_P	B32	K2	Quad 117

Table 1. FMC HA, HB, LA and High-Speed Data Pair (DP) group signal connections from Kintex-7 FPGA to FMC Site Connector J3.

Clocks and Triggers

Support for FMC integration with system devices includes clock and trigger sharing features so that multiple cards can perform simultaneous or coordinated sampling. Integration with a system timing card, such as ISI X3-Timing or Atropos, allows the cards to use common sample clocks and triggers, coordinated with GPS or another system time reference.

Most ISI FMC modules provide external clock and trigger inputs on the module's front panel. The PEX7-COP gives user an additional option for routing the external clock, trigger and 1 PPS (Pulse Per Second) signals utilizing SSMC type RF connectors. This is useful in situations where it is desirable to keep the timing signal cabling inside the host system.

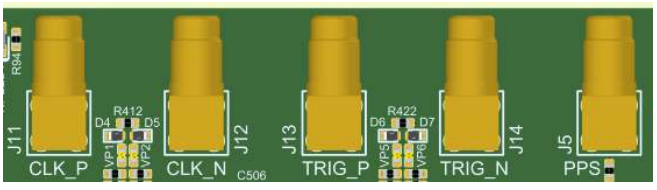


Figure 3. PEX7-COP External Timing Signal Connectors.

In default card configuration clock and trigger inputs are single ended, so connectors J11 (CLK_P) and J13 (TRIG_P) must be used.

The FMC_CLK2_BIDIR_P / MUX_FMC_CLK2_BIDIR_N signal pair used as the FMC/PEX7-COP clock signal while the FMC_CLK3_BIDIR_P / MUX_FMC_CLK3_BIDIR_N signal pair used as the FMC/PEX7-COP trigger signal. Direction of these signals is typically controlled by the FMC module itself. Additional multiplexers on both clock and trigger signals allows selection between the on-board generated and the external clock and trigger signals.

The single-ended external 1 PPM signal is buffered on the card and then connected to the FPGA pin AG9.

FPGA Core

The PEX7-COP family has a Kintex-7 FPGA and memory at its core for DSP and control. The Kintex-7 K325T FPGA has 840 DSP48E1 slices available, while K410T has 1540 DSP48E1 slices allowing implementation of advanced signal processing features. In addition to the raw processing power, the FPGA fabric integrates logic, memory and connectivity features that make the PEX7-COP capable of performing very demanding real-time signal processing.

The FPGA has direct access to the single 2048 MB DDR3 SDRAM bank configured as 256Mb x 64. This memory allows FPGA working space for computation, required by DSP functions like FFTs, as well as bulk data storage needed for system data buffering and algorithms like large FFTs. A multiple-queue controller component in the FPGA implements multiple data buffers in the DRAM that is used for system data buffering and algorithm support. The DDR3 is compatible with embedded processors (uBlaze).

The PEX7-COP uses the Kintex-7 FPGA as a system-on-chip to integrate all the features for highest performance. As such, all I/O, memory and host interfaces connect directly to the FPGA, providing direct connection to the data and control for maximum flexibility and performance. Firmware for the FPGA completely defines the data flow, signal processing, controls and host interfaces, allowing complete customization of the functionality. Logic utilization is typically <10% of the device. To maximize typical FMC module's analog converters performance, only the Clock and Trigger signals are routed outside the FPGA using components with very low jitter and skew.

FPGA Configuration

The PEX7-COP card uses a BPI FLASH memory for storing the Kintex-7 FPGA image. This FLASH can be programmed in-system from the DAQ application software.

The proper FMC module's FPGA image must be loaded into the PEX7-COP configuration flash memory BEFORE the FMC module is installed and powered up with the PEX7-COP in the system. Failure to do so may result in damage to the FMC module, PEX7-COP or both.

The FPGA JTAG interface is used for the firmware development and debugging with tools such as Xilinx Vivado and ChipScope. For JTAG programming either the built-in USB to JTAG programmer or an external programmer such as XILINX Platform USB Cable II can be used. The JTAG mode of operation is selected by the switch SW1 on the card. When the on-board USB to JTAG programmer is used, the switch must be set to "INT" (internal) position. In this case user only needs to connect a standard USB type A to micro USB cable to the micro USB receptacle J10 on the card's front panel with other end connected to any available USB port on the PC with Xilinx Vivado tool installed (which could be the same PC as the PEX7-COP card's host). If for some reason it is preferable to use an external JTAG programmer, then the SW1 switch must be set to "EXT" (external) position. The standard 14-pin ribbon cable connector from the external programmer must be plugged into the JTAG Header J1 on the PEX7-COP card.

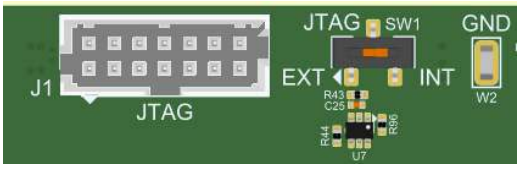


Figure 4. JTAG Mode Selection Switch SW1 and External JTAG Header J1

Communications Interfaces

The PEX7-COP host interface features the high-performance PCI Express port. This port allows the PEX7-COP to be used in many system topologies.

The PCIe port is integrated with the Velocia packet system, a powerful data network that efficiently handles data transfers between multiple, independent data sources on the PEX7-COP and the host processor. Data is packetized, using packet sizes from 32 bytes to 128KB per packet, stamped with a packet ID and destination, and then is easily routed to other devices in the system. The Velocia packet system is completely defined by the logic firmware, giving complete flexibility to create any packet routing necessary to meet system latency and transfer rate requirements.

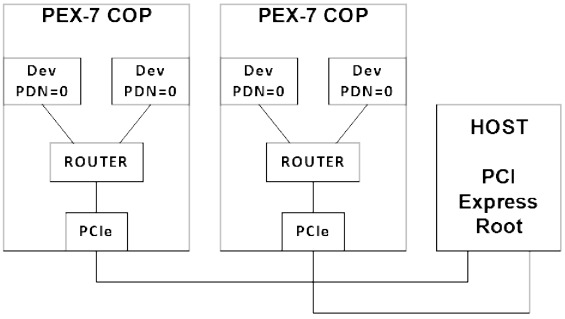


Figure 5. Example System Topology Utilizing PCIe bus

A set of logic components for packets is provided in the FrameWork Logic including packetizer, depacketizer, router and buffer memory controls. Packetizing includes timestamping per VITA 49. Data within the packets may be in any format.

Card Management and Power Features

The PEX7-COP has the hardware level power sequencing and the card health monitoring circuits to protect the system from the failure. Independent monitoring of the FPGA die temperature can shut down the card to prevent damage from overheating. In addition, the on-board system monitor circuit utilizing a precision 16-bit ADC with an analog multiplexer lets user to measure card's major voltage rails as well as the FMC module power supply currents and power consumption; the system monitor readings can be accessed from the application software.

The PEX7-COP also has a dedicated test header (J4) which allows user to manually check the voltage rails and the FMC module currents.

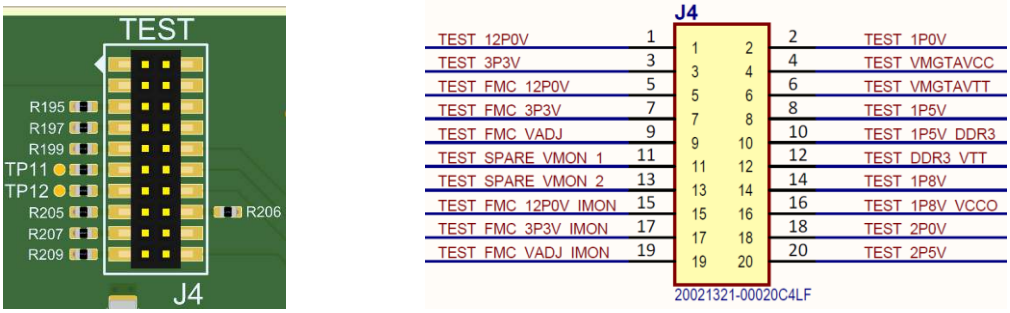


Figure 6. Test Header J4. Pin 1 marked with a white triangle.

Signal	Description / Nominal Value	Pin #		Description / Nominal Value	Signal
12P0V	System +12V; 12.0V	1	2	FPGA VCCINT; 1.0V	1P0V
3P3V	System +3.3V; 3.3V	3	4	FPGA VMGTAVCC; 1.0V	VMGTAVCC
FMC_12P0V	FMC +12V; 12.0V	5	6	FPGA VMGTAVTT; 1.2V	VMGTAVTT
FMC_ 3P3V	FMC +3.3V; 3.3V	7	8	MISC +1.5V; 1.5V	1P5V

FMC_VADJ	**FMC VADJUST, +2.5V**	**9**	**10**	**DDR3 +1.5V; 1.5V**	**1P5V_DDR3**
SPARE 1	**RESERVED**	**11**	**12**	**DDR3 TERMINATION; 0.75V**	**DDR3_VTT**
SPARE 2	**RESERVED**	**13**	**14**	**MISC +1.8V; 1.8V**	**1P8V**
FMC_12P0V_IMON*	**FMC CURRENT FROM +12V RAIL**	**15**	**16**	**FPGA VCCO +1.8V; 1.8V**	**1P8V_VCCO**
FMC_3P3V_IMON*	**FMC CURRENT FROM +3.3V RAIL**	**17**	**18**	**VCCO +2.5; 2.5V**	**2P0V**
FMC_VADJ_IMON*	**FMC CURRENT FROM VADJ RAIL**	**19**	**20**	**FPGA VCCO +2.5; 2.5V**	**2P5V**

Table 2. Test Header J4 Signals.

Note: To convert FMC Current Monitor (IMON) readings into current units use this formula:

$$I\ (A) = 5 \times Vout\ (V)$$

LED Indicators

The PEX7-COP has a few LED indicators providing user with the visual information about the card status.

LED #	Color	Function
LED 1	Red	FPGA controlled; typically indicates the host PCIe link status.
LED 2	Green	FPGA controlled; typically indicates FPGA internal status after configuration.
LED 3	Blue	FPGA "Done" – FPGA configuration successful
LED 4	Red	Card power fault indicator.
LED 5	Green	Card power good indicator.

Table 3. PEX7-COP LED Indicator Functions

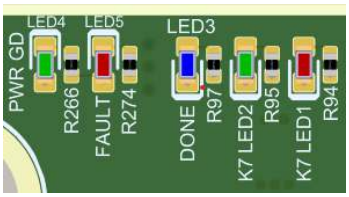


Figure 7. PEX7-COP LED Indicators

Miscellaneous Connectors and Switches

The auxiliary power connector J8 can be used to provide an additional +12V power to the card (this is not usually required). If J8 is used, it is recommended to remove the on-board jumper JP1 to prevent possible power problems if for some reason the power applied to J8 connector is different from +12V from the host PC PCIe edge connector. J8 is a commonly used 6-pin power connector with pinout compatible with a typical PC/Server power supply cabling.

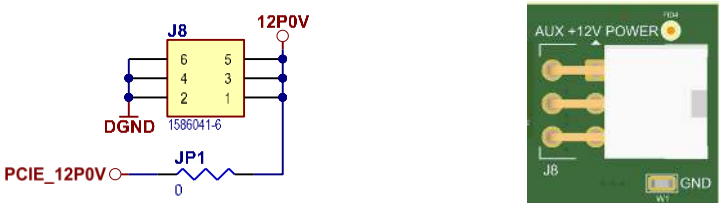


Figure 8. Auxiliary Power Connector J8. PCIE_12P0V is from the PCIe Edge connector; 12P0V is the on-board +12V power rail.

The DIP type switch SW2 allows user to set card's 3-bit geographic address accessible by the software. This feature is useful when multiple boards of the same type are used inside the same system.

Two other headers on the card - J6 (UCD9090) and J7 (SMB DEBUG) – are reserved for the factory used only.

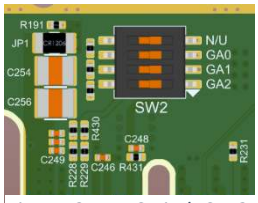
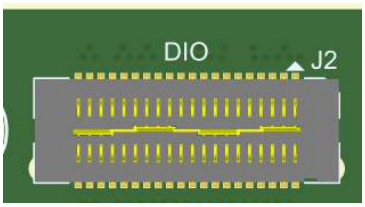


Figure 9. DIP Switch SW2 and Jumper JP1.

Digital I/O

The PEX7-COP gives user access to 28 digital I/O lines, routed as 14 tightly matched differential pairs connected to the FPGA and available on the high-speed DIO connector J2. Supported I/O standards include LVCMOS25 and LVDS25.

A breakout board with high-speed Twinax 36" cable (P/N 80350-1-L0; available separately from ISI LLC) can be used for conveniently accessing DIOs through the SMA type connectors. If it is desirable to route DIO signals outside of the host PC/server, an optional satellite daughter card (80386-0-L0) can be added. This card is essentially a simple adapter which can be plugged into any available PCIe slot (no power is required) and connected to the PEX7-COP J2 connector with a short cable. The DIO signals are routed to another connector on this card's bracket and then connected to the DIO breakout board.



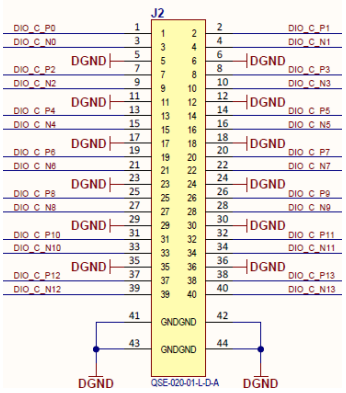


Figure 10. DIO Connector J2

PEX7-COP			80386 Satellite Card		80350 Breakout Board	
DIO SIGNAL	FPGA Pin	J2 Pin	Internal Connector J2 Pin	Bracket Connector J1 Pin	Connector J1 Pin	SMA Connector
DIO_0_P	AG24	1	1	1	1	A0_P
DIO_0_N	AH24	3	3	3	3	A0_N
DIO_1_P	AE23	2	2	2	2	B0_P
DIO_1_N	AF23	4	4	4	4	B0_N
DIO_2_P	AK20	7	7	7	7	A1_N
DIO_2_N	AK21	9	9	9	9	A2_P
DIO_3_P	AH21	8	8	8	8	B1_N
DIO_3_N	AJ21	10	10	10	10	B2_P
DIO_4_P	AG20	13	13	13	13	A3_P
DIO_4_N	AH20	15	15	15	15	A3_N
DIO_5_P	AJ22	14	14	14	14	B3_P

DIO_5_N	AJ23	16	16	16	16	B3_N
DIO_6_P	AG22	19	19	19	19	A4_N
DIO_6_N	AH22	21	21	21	21	A5_P
DIO_7_P	AF20	20	20	20	20	B4_N
DIO_7_N	AF21	22	22	22	22	B5_P
DIO_8_P	AG25	25	25	25	25	A6_P
DIO_8_N	AH25	27	27	27	27	A6_N
DIO_9_P	AK23	26	26	26	26	B6_P
DIO_9_N	AK24	28	28	28	28	B6_N
DIO_10_P	AE25	31	31	31	31	A7_N
DIO_10_N	AF25	33	33	33	33	A8_P
DIO_11_P	AJ24	32	32	32	32	B7_N
DIO_11_N	AK25	34	34	34	34	B8_P
DIO_12_P	AD21	37	37	37	37	A9_P
DIO_12_N	AE21	39	39	39	39	A9_N
DIO_13_P	AC24	38	38	38	38	B9_P
DIO_13_N	AD24	40	40	40	40	B9_N
SIGNAL GROUND	5, 6, 11, 12, 17, 18, 23, 24, 29, 30, 35, 36, 41, 42, 43, 44		5, 6, 11, 12, 17, 18, 23, 24, 29, 30, 35, 36, 41, 42, 43, 44	5, 6, 11, 12, 17, 18, 23, 24, 29, 30, 35, 36, 41, 42, 43, 44	5, 6, 11, 12, 17, 18, 23, 24, 29, 30, 35, 36, 41, 42, 43, 44	

Table 4. PEX7-COP DIO Signal Connections

Software Tools

A software development kit for the PEX7-COP provides comprehensive support including device drivers, data buffering, card controls, and utilities that allow developers to be quickly productive. At the most fundamental level, the software development kit delivers data buffers to your application without the burden of low-level real-time control of the card. Software classes provide C++ developers a powerful, high level interface to the card that makes real-time, high-speed data acquisition easier to integrate into applications. Qt Creator project files are provided to compile and build C/C++ applications on 64-bit Windows or Linux operating systems. For additional help please contact technical support.

The provided *Athena* software package allows use of the PEX7-COP card straight out of the box. The *DAQ* application provides card configuration, dynamic waveform generation, system monitoring, and logic reconfiguration. The *Binview* utility provides data viewing, analysis, and export capability to other software packages.

Logic Tools

The FrameWork Logic tools support RTL development. The standard logic provides a hardware interface layer that allows designers to concentrate on the application-specific portions of the design. Designers build upon the ISI components for data handling, hardware interfaces and system functions, the Xilinx IP core library, and third party IP. RTL source for the FrameWork Logic is available separately and can be used for customization.

The FrameWork Logic User Guide provides more detail.

PEX7-COP

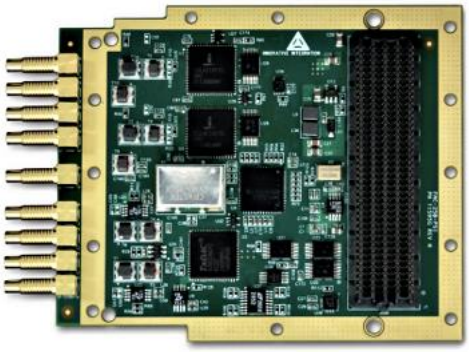
FMC Modules

ISI offers variety of FMC modules which can be used along with the PEX7-COP to build a custom high-performance system. All ISI FMC modules work at Vadj=2.5V, which is the default value on the PEX7-COP. In addition, most of the ISI FMC modules are capable of operation within a wider Vadj range providing more flexibility for the system designers.

FMC-250 (80315)

FMC Module with Two 250 MSPS 16-bit ADCs, Two 1200 MSPS 16-bit DACs with PLL and Timing Controls

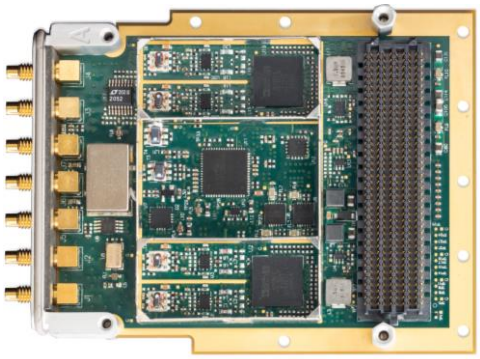
Vadj = 2.5V (1.8V to 2.5V supported)



FMC-310 (80320)

FMC Module with Four 310 MSPS 16-bit ADCs with PLL and Timing Controls

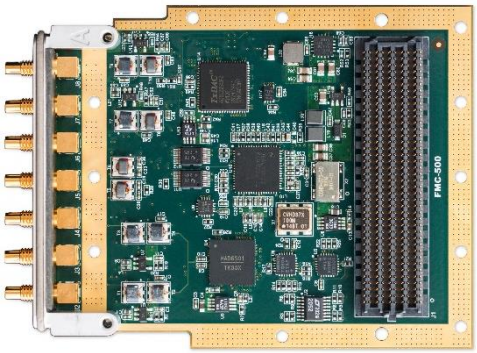
Vadj = 2.5V



FMC-500 (80281)

FMC Module with Two 500 MSPS 14-bit ADCs, Two 1200 MSPS 16-bit DACs with PLL and Timing Controls

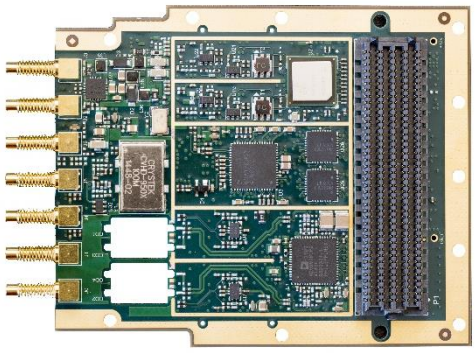
Vadj = 2.5V (1.8V to 2.5V supported)



FMC-1000 (80325)

FMC Module with Two 1000 or 1250 MSPS 14-bit ADCs, Two 1230 MSPS 16-bit DACs with PLL and Timing Controls

Vadj = 2.5V



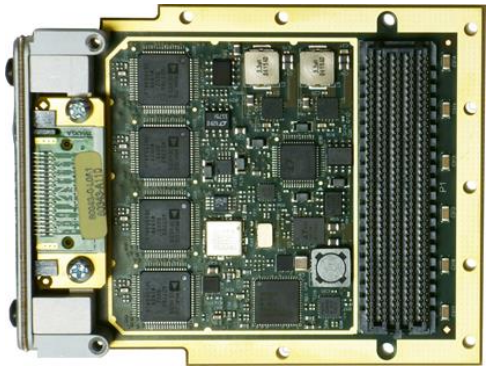
PEX7-COP

INTERCONNECT SYSTEMS
a molex company

FMC-SDF (80358)

FMC Module with Four 24-bit, 625 kSPS ADC Channels; Two 18-bit DAC Channels with on-board Timing Controls and Tachometer

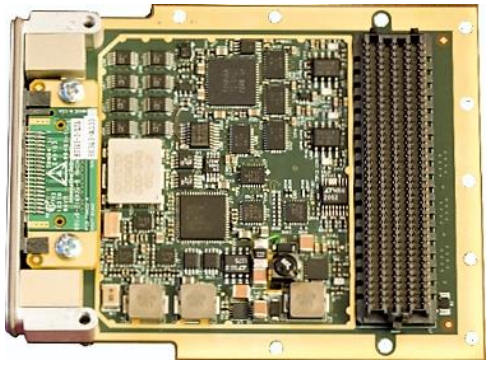
Vadj = 2.5V (1.8V to 2.5V supported)



FMC-Servo (80339)

FMC Module with Eight 16-bit, 500 kSPS ADC Channels; Eight 16-bit DAC Channels with on-board Timing Controls

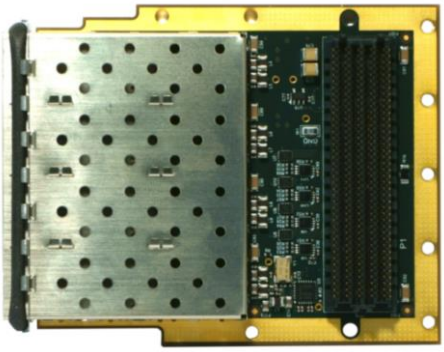
Vadj = 2.5V (1.8V to 2.5V supported)



FMC-SFP+ (80285)

FMC Module with Four SFP+ Ports

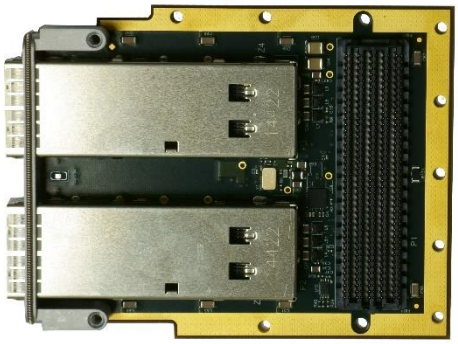
Vadj = 2.5V (1.8V to 2.5V supported)



FMC-QSFP+ (80289)

FMC Module with Two QSFP+ Ports

Vadj = 2.5V (1.8V to 2.5V supported)



PEX7-COP

Usage and Market

The PEX7-COP is a digital device and apparatus exclusively for use in business, industrial and commercial environments. The PEX7-COP peripheral is not marketed, sold or otherwise made available for home or residential environment use.

The PEX7-COP is exclusively for use with wired input and output signals. The PEX7-COP peripheral is not an intentional radio transmitter or receiver and is not marketed, sold or otherwise made available for connection to wireless media (with an antenna, etc.).

The PEX7-COP is not a “PC” (“personal” or “portable computer” marketed for home or residential environment use) or “PC” peripheral and is not marketed, sold or otherwise made available as a “PC” or “PC” peripheral.

The PEX7-COP may be sold as a subassembly where the integrator/purchaser takes responsibility for their assembled digital device’s or apparatus’s compliance. Consult ISI/Molex for clarification and assistance.

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