X6-1000M

V 1.8 7/17/20

INTERCONNECT SYSTEMS
a molex company

XMC Module with 2x 1 GSPS 12-bit A/D, 4x 500 MSPS/2x 1 GSPS 16-bit DAC, Virtex6 FPGA, 4GB Memory and PCI Express

FEATURES

- Two 1 GSPS, 12-bit A/D channels
- Four 500 MSPS or two 1 GSPS 16-bit DACs
- 2Vpp, AC or DC -Coupled, 50 ohm, SSMC inputs
- 1Vpp, AC or DC -Coupled, 50 ohm, SSMC outputs
- Xilinx Virtex6 SX475T
- 4 Banks of 1GB DRAM (4 GB total)
- Ultra-low jitter programmable clock
- Arbitrary Waveform Generation Memory Controller for DACs
- Gen2 x8 PCI Express providing over 2.8 GB/s sustained transfer rates
- XMC Module (75x150 mm)
- 31W typical
- Conduction Cooling per VITA 20
- Ruggedization Levels for -40 to 85C and 0.1 g^2/Hz vibration/ 40g shock environments
- Adapters for PCIe, VPX, Compact PCI, desktop PCI and cabled PCI Express systems

APPLICATIONS

- Wireless Receiver
- WLAN, WCDMA, WiMAX front end
- RADAR
- Medical Imaging
- High Speed Data Recording and Playback
- IP development

SOFTWARE

- VHDL FrameWork Logic
- Windows/Linux Drivers
- C++ DevKit

DESCRIPTION

The X6-1000M integrates 1 GSPS data conversion with high performance signal processing on an XMC IO module for demanding DSP applications. The tight coupling of the data converters to the Virtex6 FPGA core realizes architectures for SDR, RADAR, and LIDAR front end sensor digitizing and processing. The PCI Express system interface sustains transfer rates over 2.8 GB/s for data recording and integration as part of a high performance real-time system.

The X6-1000M features two, 12-bit, 1 GSPS A/Ds, and four, 16-bit, 500 MSPS DACs. The DAC channels may also be configured as two, 16-bit, 1 GSPS outputs. An Analog input bandwidth of over 2 GHz supports wideband and undersampling applications. The DACs feature interpolation and coarse mixing functions for upconversion. Precise synchronization features insure exceptional DAC output phase alignment. The sample clock is sourced from a low-jitter PLL or an external clock/reference. Multiple boards offer coherent sampling as well as up and down-conversion.

A Xilinx Virtex-6 SX475T with 4 banks of 1GB DRAM provides a very high performance DSP core with over 2000 MACs. The close integration of the analog IO, memory and host interface with the FPGA enables real-time signal processing at extremely high rates.

The X6-1000M power consumption is 28W for typical operation. The module may be conduction cooled using VITA20 standard and a heat spreading plate.

The X6-1000M FPGA design can be fully customized using VHDL and the FrameWork Logic Devkit.

A software development kit for host development includes C++ libraries and 64-bit drivers for Windows and Linux. An application demonstrating the module's features, including streaming DAC samples from disk, is provided.

XILINX®

X6-1000M

This electronics assembly can be damaged by ESD. Innovative Integration recommends that all electronic assemblies and components circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very SSMCll parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

Product	Part Number	Description
X6-1000M		PMC/XMC module with two 1 GSPS A/Ds, two 1 GSPS or four 500 MSPS 16-bit DACs, Virtex-6, 4GB DRAM.
	80280-0-L0	X6-1000M with LX240T FPGA, DC-coupled inputs
	80280-1-L0	X6-1000M with LX240T FPGA, AC-coupled inputs
	80280-2-L0	X6-1000M with SX315T FPGA, -1 speed. DC -coupled inputs
	80280-3-L0	X6-1000M with SX315T FPGA, -1 speed. AC -coupled inputs
	80280-5-L0	X6-1000M with SX475T2 FPGA, -2 speed. DC -coupled inputs
	80280-6-L0	X6-1000M with SX315T FPGA, -2 speed. AC -coupled inputs
	80280-8-L0	X6-1000M with SX475T2 FPGA, -2 speed. AC -coupled inputs
	80280-10-L0	X6-1000M with SX315T2 FPGA, DC -coupled inputs
	80280-11-L0	X6-1000M with LX240T2 Speed 2 FPGA, AC -coupled
	80280-12-L0	X6-1000M with LX240T2 Speed 2 FPGA, DC -coupled inputs
	80280-14-L0	X6-1000M with SX475T2 FPGA, PCIe 8-lane gen2, AC coupled in DC coupled out
		Environmental Rating -L1, -L2, -L3 or -L4 available upon request.
X6-1000M FrameWork Logic	55037	X6-1000M FrameWork Logic board support package for RTL and MATLAB. Includes technical support for one year.
Cables		
SSMC to BNC cable	67156	Coax cable with SSMC (plug) to BNC (female), 1 meter
Adapters		
XMC-PCIe x8 Adapter	80363	PCI Express carrier board for XMC modules, x8 lanes, Onboard USB JTAG, Robust Thermal Solution, Voltage Monitor, 8 high quality Differential DIO pairs, High speed expansion port (QSFP)
XMC-PXIe Adapter	80341	PXIe carrier carrier board for XMC modules, x8 lanes, 8 High Speed gigabit transceiver (QSFP), 8 high quality Differential DIO pairs
XMC-PCIe Adapter	80259	PCI Express carrier board for XMC modules, x8 lanes, JN4 connector with 32 standard Differential DIO pairs
XMC-compact PCI/PXI Adapter	80207	3U compact PCI carrier board for XMC modules, 64-bit PCI. Support for PXI clock and trigger features (logic dependent).
DAQ Node	90181	Cabled PCI Express carrier board, x1 lane, XMC enclosure
3U VPX Adapter	80260	VPX carrier board for XMC modules, x4 lanes, Conduction-cooled, DIO configurable for JN4 or P16 connector

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Embedded PC Host		
ePC-Duo	90602 See datasheet for options	ePC-Duo: Carrier Board for x2 XMC module, x8 lane, Skylake Processor, 32GB RAM, x1 1 Gbe, x2 10 Gbe, x4 mSATA, IEEE or GPS optional, x2 QSFP ports, Onboard USB JTAG (XMC module must have JTAG signals on P16 XMC connector), onboard voltage monitor, x10 high quality XMC module DIO pairs from each XMC module, convection-cooled chassis, 150W power supply
SBC-Nano	90654-0-L0	SBC-Nano: Carrier Board for x1 XMC module, COM Express Type 10 ATOM, 8 GB DDR3L memory, x4 lanes PCIe, x2 mSATA, x1 Gbe, Conduction or Convection cooled chassis
VPXI-ePC	90271-0	VPXI System – 3U VPX embedded PC system with 4 expansion slots; runs Windows, Linux, or VxWorks; Intel i7 CPU, integrated timing support backplane
Heatsinks		
Standard Adapter (VPX, PXIe, DAQ-Node, eInstrument-PC, XMC-PCIe Adapter)	61548-1	Assembly, Heatsink Hardware, X6, XA on PXIe, VPX, ePC, DAQ-Node, XMC-PCIe Adapter
Standard Adapter (ePC-Duo)	Not Needed	EPC-Duo has the correct heatsinks installed.
Standard Adapter (SBC-Nano)	61543-1	Assembly, Heatsink Hardware, X6, XA on ePC-Nano

Note: <ER> corresponds to -L0, -L1, -L2, -L3 or -L4 rating from Operating Environment Table below.

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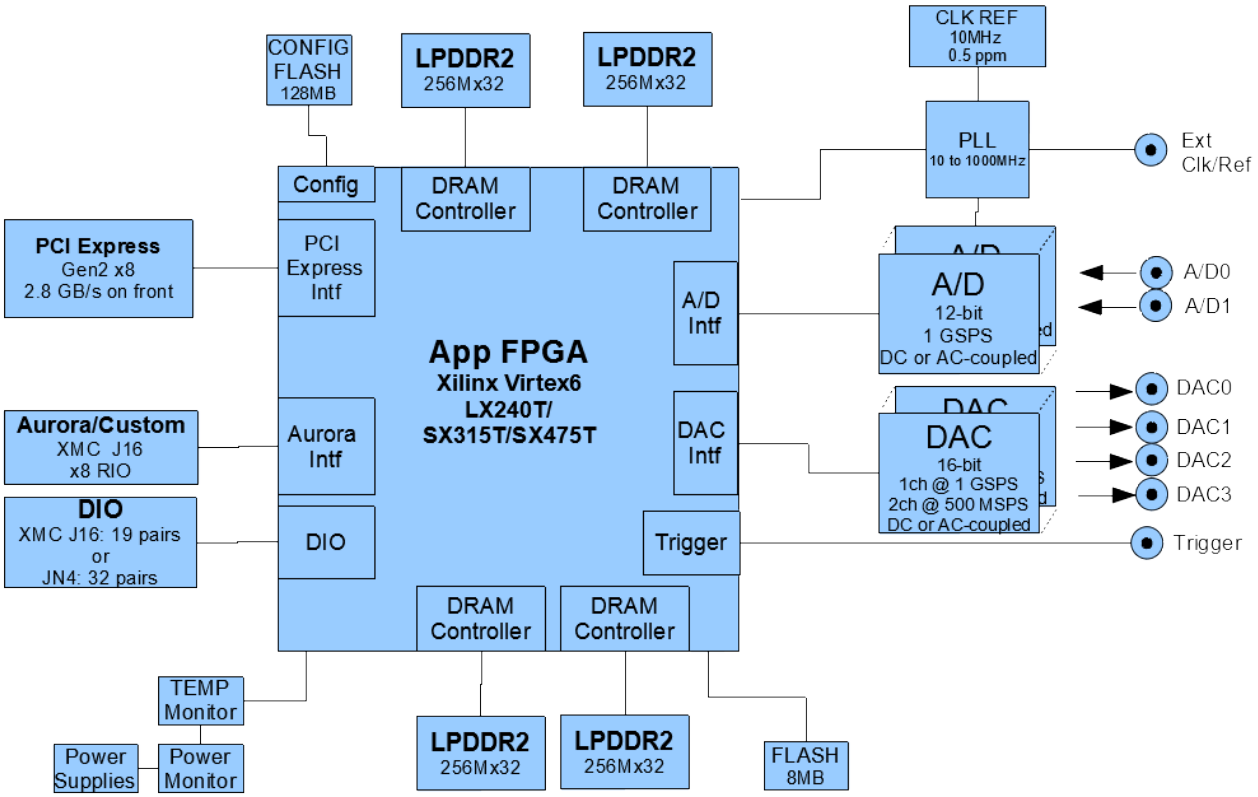
X6-1000M Block Diagram



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Operating Environment Ratings

X6 modules may be qualified for wide temperature, vibration and shock environmental ratings to suit a variety of applications.

Minimum lot sizes and NRE charges may apply. Contact ISI sales (ISIsales@molex.com) for pricing and availability.

X6-1000M

Standard Features

Analog Inputs	
Inputs	2
Input Range	2Vpp
Input Type	Single ended, AC or DC coupled
Input Impedance	50 ohm
A/D Device	Texas Instruments ADS5400
A/D Resolution	12-bit
A/D Sample Rate	100 MHz to 1 GHz
Analog Outputs	
Outputs	4 channels Configurable as 2 channels at double rate
Output Range	1 Vpp
Output Type	Single ended, AC or DC coupled
Output Impedance	50 ohm
DAC Device	2x Texas Instruments DAC5682Z
DAC Resolution	16-bit
DAC Update Rate	250 MHz to 1 GHz

FPGA	
Devices	Xilinx Virtex6 SX475T
Speed Grades	-1, -2
Logic Cells	LX240T: 241,152 SX315T : 314,880 SX475T: 476,160
Multipliers	LX240T: 768 SX315T: 1344 SX475T: 2016
Slice	LX240T: 37680 SX315T: 49200 SX475T: 74400
Block RAMs	LX240T: 832 (14976 Kbiits) SX315T: 1408 (25344 Kbits) SX475T: 2128 (38304 Kbits)
Rocket IO	16 lanes @ 5 Gbps (-1 speed)
Configuration	JTAG or FLASH In-system reprogrammable

Memories	
DRAM Size	4 GB; 4 banks of 1GB each
DRAM Type	LPDDR2 DRAM
DRAM Controller	Controller for DRAM implemented in logic. DRAM is controlled as a single bank.
DRAM Rate	3.2 GB/s transfer rate per bank (400 MHz clock)

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Host Interface	
PCI Express	x8 Lanes, VITA 42.3 PCI Express Gen 2 (x4 for -1 speed FPGA) PCI Express Gen 1 (x8)
PCI Express Sustained Rate	3.0 GB/s (x8 Gen2)

Clocks and Triggering	
Clock Sources	PLL or External
	PLL: 10 to 1000 MHz, and integer divisions thereof External: 250 to 1000 MHz
PLL Reference	External or 10MHz on-board 10MHz ref is +/-250ppb -40to 85C
PLL Resolution	100 kHz tuning resolution (default)
Phase Noise	-130 dBc @ 100 kHz
Triggering	External, software, acquire N frame, Repeated Interval
Ext Trigger Timing	Risetime < 1.0 uS
Ext Trigger Level	0.5 – 2.5 Vpp
Decimation	1:1 to 1:4095 in FPGA
Channel Clocking	All channels are synchronous
Multi-board Synchronization	External triggering input is used to synchronize sample clocks or an external clock and trigger may be used.
Transport Delay	ADC: 40 fs clock samples DAC: 94 fs clock samples
Monitoring	
Alerts	Trigger Start, Trigger Stop, Queue Overflow, Channel Over-range, Timestamp Rollover, Temperature Warning, Temperature Failure
Alert Timestamping	5 ns resolution, 32-bit counter

Application IO (J4/J16)	
Gigabit Serial Lanes	8 Tx/Rx pairs (J16)
Gigabit Serial data rate	5 Gbps/lane full duplex
DIO Bits, total	32 (J16/J4)
Signal Standard	LVCMOS (2.5V) – NOT 3.3 compatible
Drive	+/-12 mA
Connectors	PMC JN4/ XMC J16

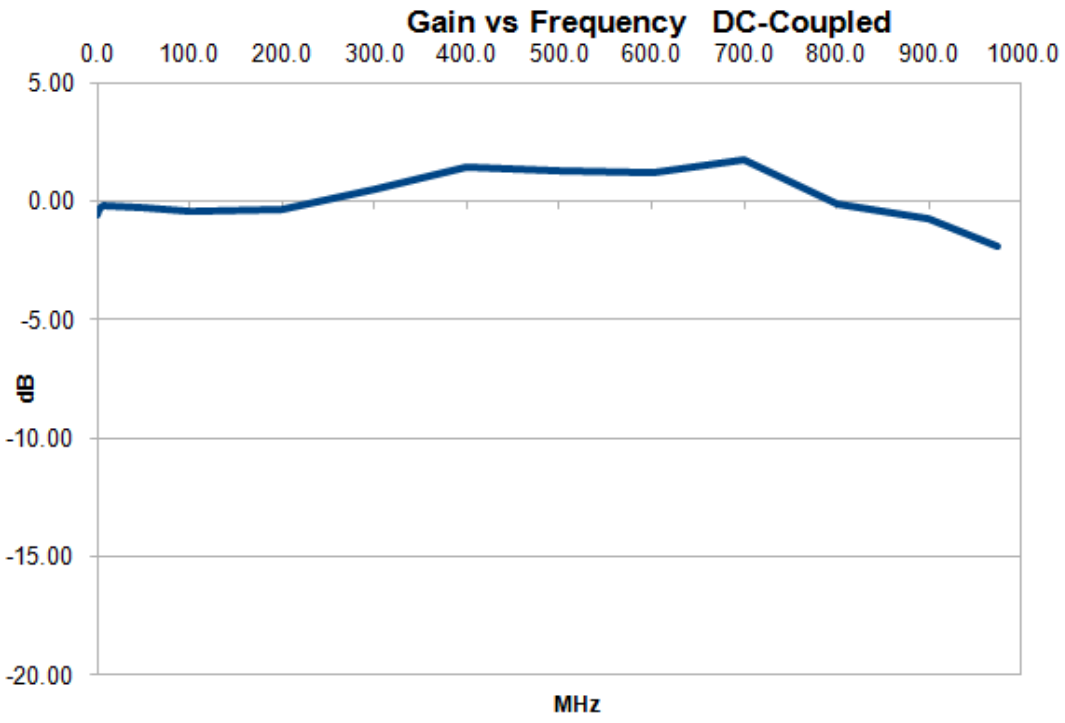
Power	
Consumption	28W (VPWR = 5V, 1 DDR bank and no Aurora ports instantiated, 4 lane PCIe) 33W (VPWR = 12V, 4 DDR banks, all Aurora ports, 8 lane PCIe)
Temperature Monitor	Software with programmable alarms
Over-temp Monitor	Disables power supplies
Power Control	Channel enables and power up enables
Heat Sinking	Conduction cooling supported (VITA20 subset)

Physicals	
Form Factor	Single width IEEE 1386 Mezzanine Board
Size	75 x 150 mm
Weight	130g
Hazardous Materials	Lead-free and RoHS compliant

X6-1000M

ELECTRICAL CHARACTERISTICS At 24C ambient.			
Parameter	Typ	Units	Notes
A/D Performance – AC coupled			
Analog Input Bandwidth (AC Coupled) Analog Input Bandwidth (DC Coupled)	750 1098	MHz MHz	-3dB -3dB
SFDR	68	dB	71 MHz sine input, 85%FS, Fs = 1 GSPS
S/N	55	dB	71 MHz sine input, 85%FS, Fs = 1 GSPS
THD	-67	dB	71 MHz sine input, 85%FS, Fs = 1 GSPS
ENOB	8.9	bits	71 MHz sine input, 85%FS, Fs = 1 GSPS
Channel Crosstalk	<-100	dB	71 MHz sine input, 9dBm adjacent channel input, Fs = 1 GSPS
Noise Floor	-103	dB	Input grounded, Fs = 1 GSPS, 64K sample FFT, non-averaged
Gain Error	<0.2	% of FS	Calibrated
Offset Error	<1	mV	Calibrated
A/D Performance – DC Coupled			
Analog Input Bandwidth	1000	MHz	-3dB
SFDR	58	dB	71 MHz sine input, 85%FS, Fs = 1 GSPS
S/N	55.1	dB	71 MHz sine input, 85%FS, Fs = 1 GSPS
THD	-57	dB	71 MHz sine input, 85%FS, Fs = 1 GSPS
ENOB	8.6	bits	71 MHz sine input, 85%FS, Fs = 1 GSPS
Channel Crosstalk	<-98	dB	71 MHz sine input, 9dBm adjacent channel input, Fs = 1 GSPS
Noise Floor	-101	dB	Input grounded, Fs = 1 GSPS, 64K sample FFT, non-averaged
Gain Error	<0.2	% of FS	Calibrated
Offset Error	<1	mV	Calibrated
DAC Performance – AC Coupled			
Analog Output Bandwidth	1000	MHz	
SFDR	64.5	dB	71 MHz sine output, AC coupled
S/N	62	dB	71 MHz sine output, AC coupled
THD	-61.6	dB	71 MHz sine output, AC coupled
ENOB	9.5	bits	71 MHz sine output, AC coupled

Channel Crosstalk	<-85	dB	Aggressor = 125.1 MHz, -3 dBfs adjacent channel
Gain Error	<0.2	% of FS	Calibrated
Offset Error	<500	µV	Calibrated
DAC Performance – DC Coupled			
Analog Output Bandwidth	600	MHz	
SFDR	65	dB	71 MHz sine output, -6 dBfs, DC coupled
S/N	56	dB	71 MHz sine output, -6 dBfs, DC coupled
THD	-65	dB	71 MHz sine output, -6 dBfs, DC coupled
ENOB	9.1	bits	71 MHz sine output, -6 dBfs, DC coupled
Channel Crosstalk	<-85	dB	Aggressor = 71 MHz, -3 dBfs adjacent channel
Gain Error	<0.2	% of FS	Calibrated
Offset Error	<500	µV	Calibrated



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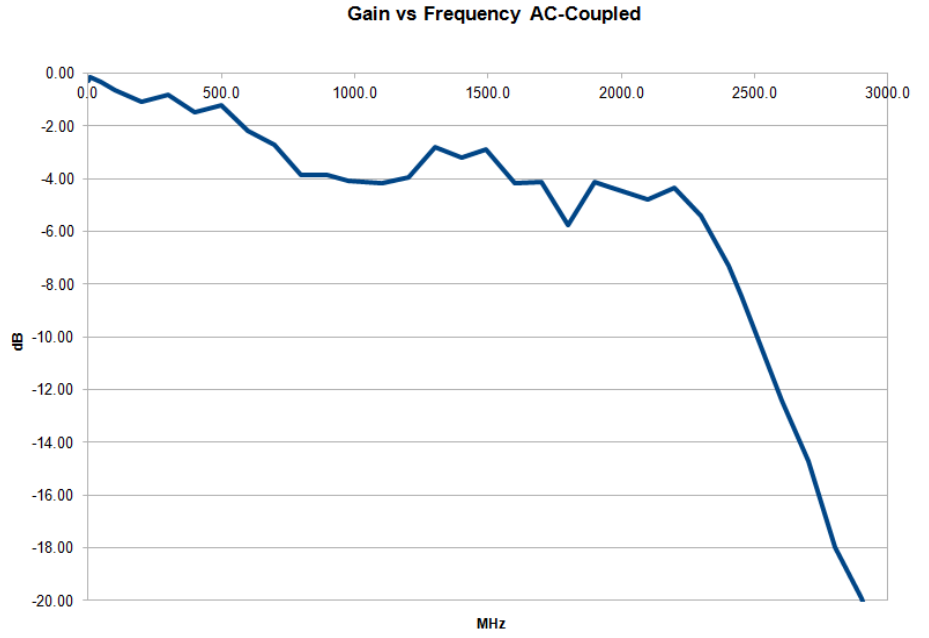
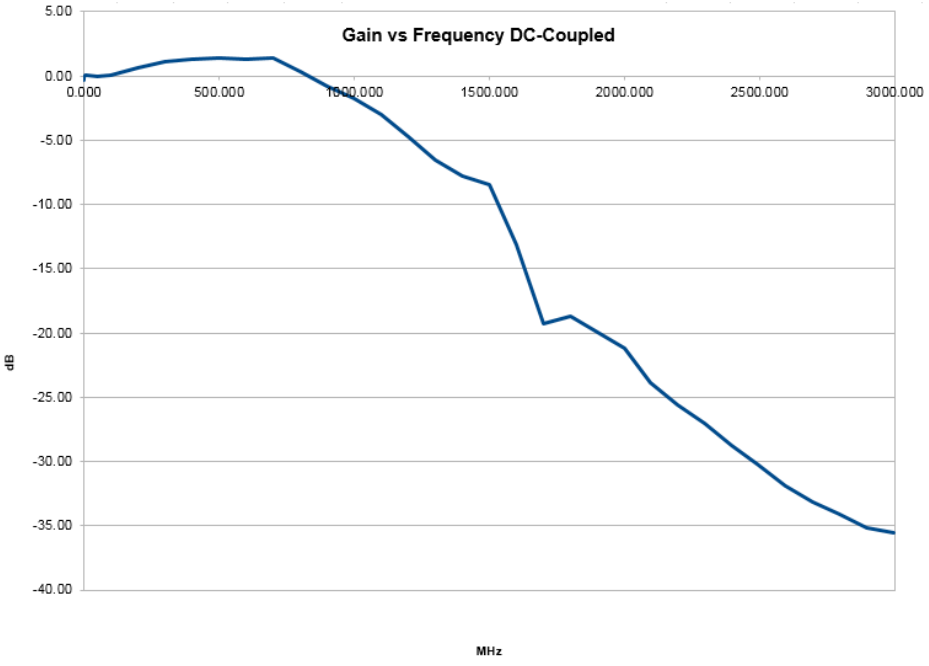

Gain vs Frequency AC-Coupled
0.00
-2.00
-4.00
-6.00
-8.00
-10.00
-12.00
-14.00
-16.00
-18.00
-20.00
dB
0.0
500.0
1000.0
1500.0
2000.0
2500.0
3000.0
MHz


Gain vs Frequency DC-Coupled
5.00
0.00
-5.00
-10.00
-15.00
-20.00
-25.00
-30.00
-35.00
-40.00
dB
0.000
500.000
1000.000
1500.000
2000.000
2500.000
3000.000
MHz

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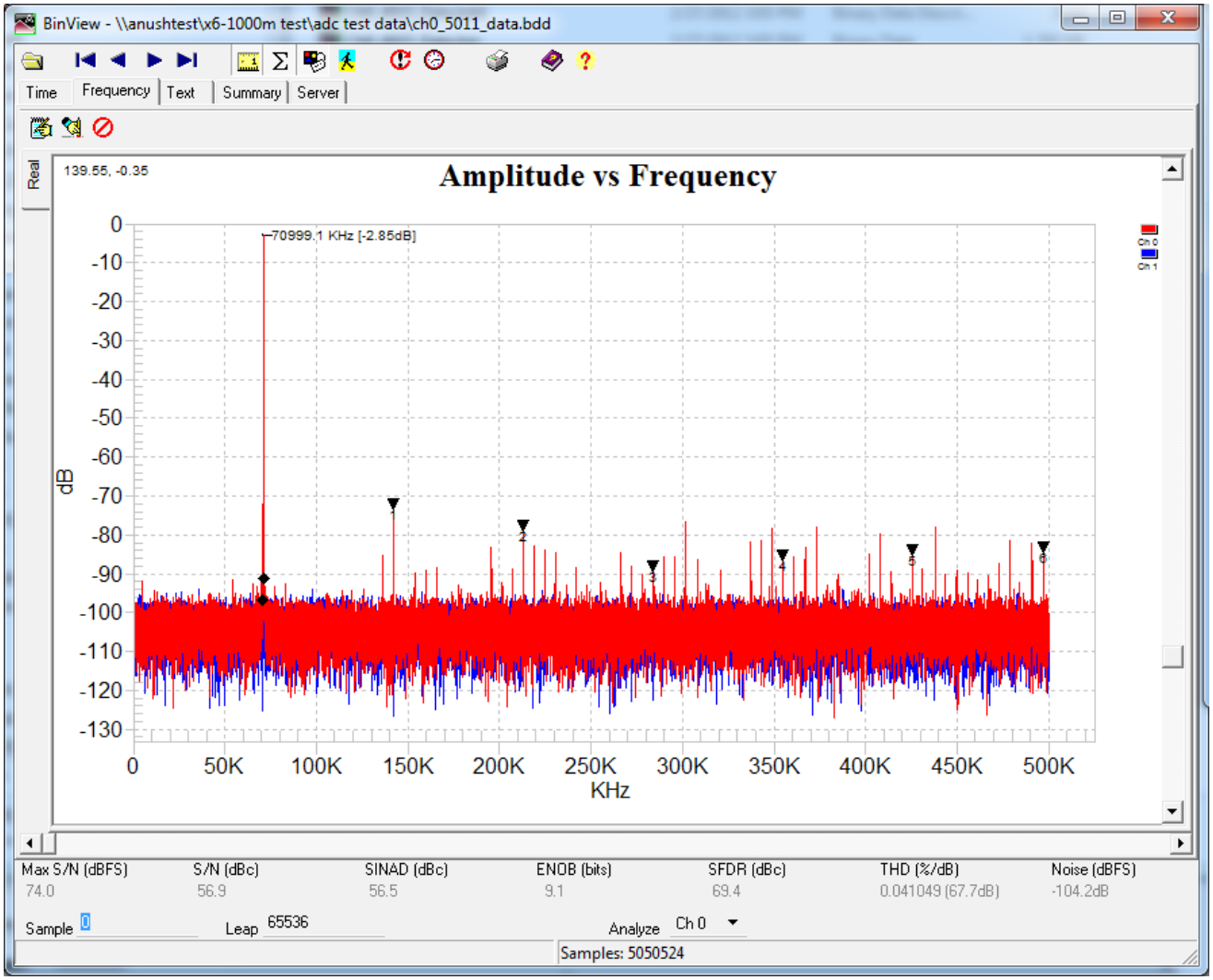

A/D Signal Quality: AC-coupled input, Fs = 1000MHz, Fin = 71 MHz, -3 dBfs

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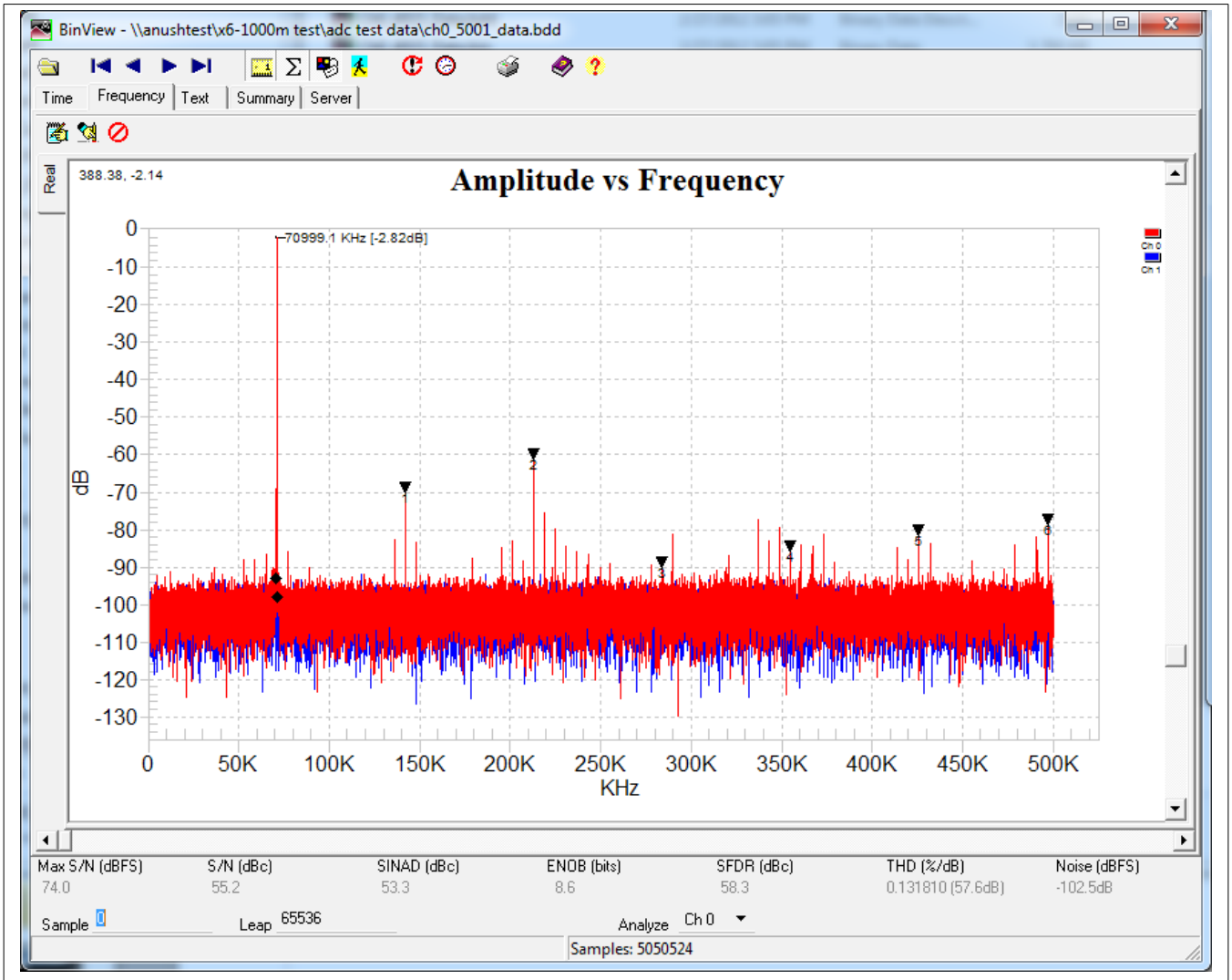
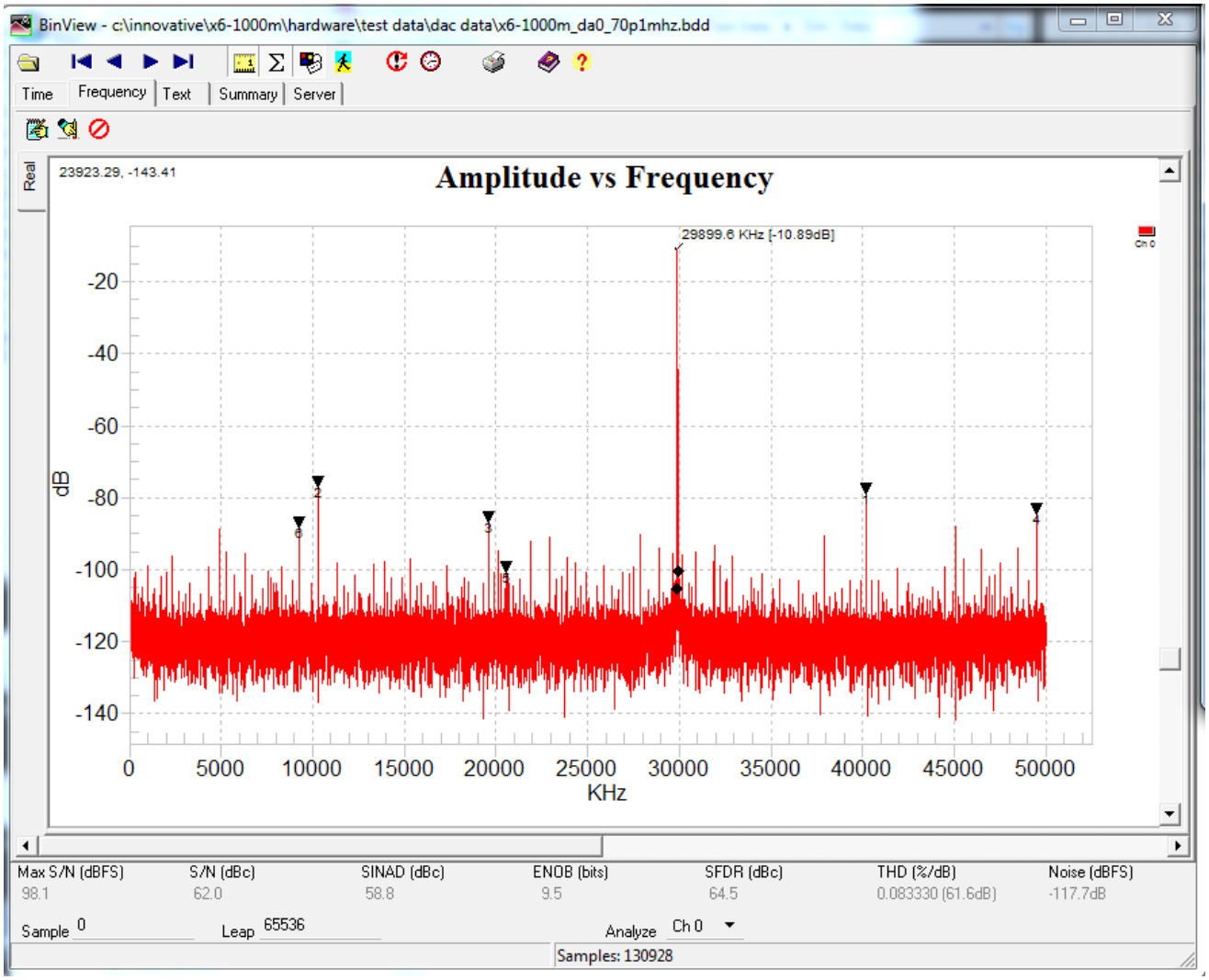


A/D Signal Quality: DC-coupled input, Fs = 1000MHz, Fin = 71 MHz, -3 dBfs



DAC AC-Coupled Signal Quality: Fs = 500MHz, Fout = 70.1 MHz, 1Vp-p

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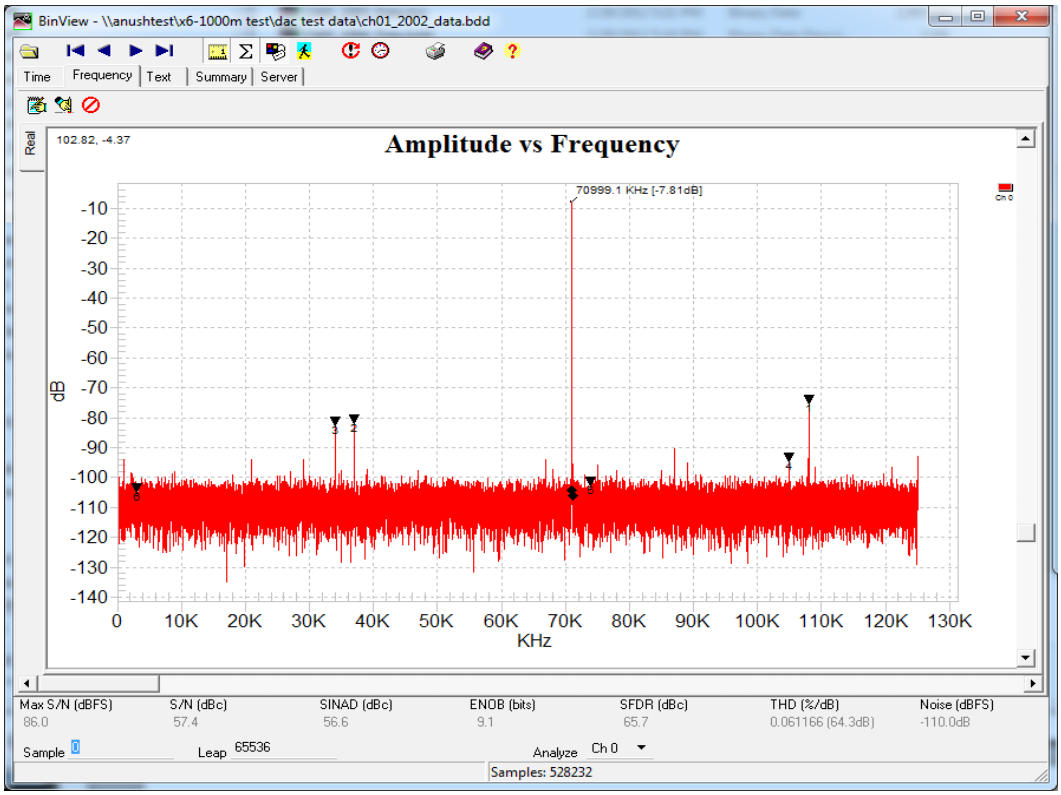


DAC DC-Coupled Signal Quality: Fs = 500MHz, Fout = 71 MHz, 1Vp-p

Architecture and Features

The X6-1000M module architecture integrates analog IO with an FPGA computing core, memories and PCI Express host interface. This architecture tightly couples the FPGA to the analog signals for real-time signal processing with low latency and extremely high rates. The X6-1000M is an ideal front-end for demanding applications in wireless, RADAR and medical imaging applications.

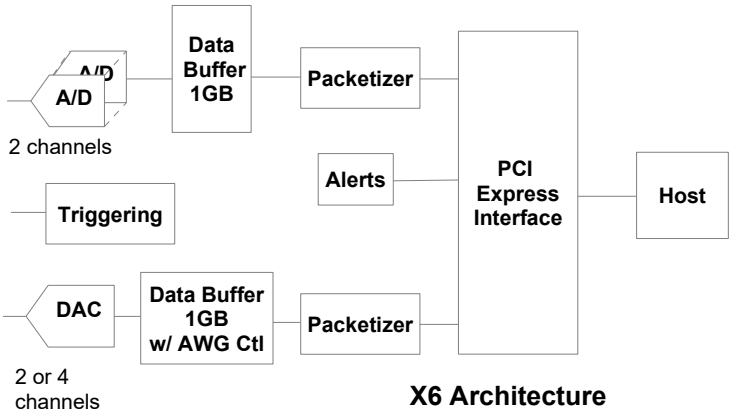
X6-1000M

Analog IO

The analog front end of the X6-1000M module has two simultaneously sampling channels of 12-bit, 1 GSPS A/D input and four channels of 500 MSPS or two channels of 1 GSPS 16-bit DAC output. The A/D inputs have an analog input bandwidth of 2 GHz for wideband and direct sampling applications.

The A/Ds are directly connected to the FPGA for minimum data latency. In the stock X6-1000M Framework Logic, the A/Ds have an interface component that receives the data, performs digital calibration correction, and provides a FIFO memory for data buffering. A non-volatile ROM on the module stores factory-programmed, unique calibration coefficients for each data converter.

Data flow between the IO and the host using a packet system



X6 Architecture

The DACs are sourced directly from the FPGA with support for host data streaming over the PCIe bus or for arbitrary waveform generation (AWG) from the FPGA. In the AWG mode, a memory controller plays a dynamically linked list of data buffers residing in memory to the DAC at rates up to 1 GSPS (dual DAC configuration). The data buffers, along with their playback parameters are supplied by the host via PCIe or by the FPGA firmware. The playback parameters include gain level, number of repetitions to play, next buffer to play, and playback termination methods.

A flexible set of trigger configuration modes, fully integrated with the FPGA logic, allows precise control over data acquisition and playback. Trigger start is initiated by an external trigger signal or via software command. Triggering may be specified as either edge or level sensitive, dependent on the source, and may be optionally programmed with user-defined frame sizes and repeat intervals. Multiple modules sample synchronously when the external trigger inputs are used with a common trigger signal. The trigger component in the FPGA VHDL is user-customizable to accommodate a variety of triggering requirements.

FPGA Core

The X6 Module family has a Virtex6 FPGA and memory at its core for DSP and control. The Virtex6 SX475T FPGA contains over 2000 DSP elements. In addition to raw processing power, the FPGA fabric integrates logic, memory and connectivity features that make the FPGA capable of applying this processing power to virtually any algorithm with sustained performance in real-time. The FPGA has direct access to four banks of 1GB DRAM. These memories allow the FPGA working space for computation, required by DSP functions like FFTs, and bulk data storage needed for system data buffering and algorithms like Doppler delay. A multiple-queue controller component in the FPGA implements multiple data buffers in the DRAM.

The X6 module family uses the Virtex6 FPGA to integrate the module's components for highest performance. As such, all IO, memory and host interfaces connect directly to the FPGA – providing direct connection to the data and control for maximum flexibility and performance. Firmware for the FPGA completely defines the data flow, signal processing, controls and host interfaces, allowing complete customization of the X6 module functionality. FPGA resource utilization is typically <10% of the device.

PCI Express Host Interface

The X6 architecture delivers over 2.8 GB/s sustained data rates over PCI Express using the Velocia packet system. The Velocia packet system is an application interface layer on top of the fundamental PCI Express interface that provides

efficient and flexible DMA transfers at high data rates with minimal host support. The packet data system controls the flow of packets to the host, or other recipient, using a credit system managed in cooperation with the host software. The packets may be transmitted continuously for streams of data from the A/Ds, or as occasional packets for status, controls and analysis results. For all types of applications, the data buffering and flow control system delivers high throughput with low latency and complete flexibility for data types and packet sizes to match the application requirements. Firmware components for assembling and dissembling packets are provided in the FrameWork Logic which allow applications to rapidly integrate data streams and controls into the packet system with minimum effort.

System Data Plane Ports and Digital IO

The X6 module family has eight high speed serial data links on XMC connector J16 for system interconnect, operating at up to 5 Gbps per link, full duplex. These links enable the X6 modules to integrate into switched fabric systems such as VPX to create powerful computing and signal processing architectures. The standard Framework Logic implements these lanes as two Aurora ports of 4 lanes each. Other protocols such as SRIO and SFPDP may be implemented in the FPGA.

32 general purpose digital IO lines are available via JN4 connector. These lines connect directly to the FPGA.

Module Management

The X6 family has independent temperature monitoring for the FPGA die. The temperature sensor is set so that power shuts when a critical temperature is exceeded. This function is independent of the FPGA.

The data acquisition process can be monitored using the module alert mechanism. The alerts provide information on the timing of important events such as triggering, overranges and thermal overload. Packets containing data about the alert include an absolute system timestamp of the alert, and other information such as current temperature. This provides an overview of the module's data acquisition process by recording the occurrence of these real-time events making the module easier to integrate into larger systems.

FPGA Configuration

The module uses a FLASH memory for the Virtex 6 FPGA image. This FLASH can be programmed in-system using a software applet. There are two images in the FLASH: an application image and a "golden" image as a backup.

During development, the JTAG interface to the FPGA is used for development tools such as ChipScope and MATLAB. The FPGA JTAG connector is compatible with Xilinx Platform USB Cable.

Software Tools

Software development tools for the module provide comprehensive support including device drivers, data buffering, module controls, and utilities that allow developers to be productive. At the most fundamental level, the software library components deliver data buffers to the top-level application without the burden of low-level, real-time control of the module and its interface. Software classes provide C++ developers a powerful, high-level interface to the module that makes real-time, high speed data acquisition easier to integrate into applications.

Software for data logging and analysis are provided with every module. Data can be logged to system memory at full rate or to disk drives at rates supported by the drive and controller. Triggering and sample rate controls allow you to use the module's feature with a supplied application without ever writing code. Software applets include *Binview* which provides data viewing, analysis and import to MATLAB for large data files.

Support for the QtCreator and GNU C++ toolchains are provided. Microsoft Visual Studio toolchain is available by request. Supported OS's include Windows and Linux. For more information, the software tools User Guide and on-line help is available by request, contact Tech Support (ISItechsupport@molex.com).

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Logic Tools

Custom DSP applications may be readily included in the module's FPGA. The standard Framework Logic provides a hardware interface layer that allows designers to concentrate on the application-specific portions of the design. Designer can build upon the supplied components for packet handling, hardware interfaces and system functions, the Xilinx IP core library, and third party IP. RTL source for the FrameWork Logic is provided for customization. Each design is provided as a Xilinx ISE project,.

The FrameWork Logic User Guide more fully detail the development tools. Some of the more important logic functions are shown here.

Logic Core	Description	Features
PCIe Interface	Interface to PCI Express bus supporting x1 to x8 lanes, Gen1 or Gen2. Implements Velocia packet system and Wishbone SOC bus.	Supports sustained data rates of up to 2.8 GB/s. Automates DMA transfers to the system using Velocia packet protocol. Wishbone SOC bus provides flexible bus architecture for designers.
Aurora Interface	Interface to x4 Aurora port for system expansion and data communications.	Provides up to 2.5 GB/s data port to other modules for system expansion and data plane integration. Sub-channel support for messaging.
Router	Velocia packet router.	Dynamically steers packets amongst source and destination logic components.
Packetizer	Creates Velocia or VITA 49 packets.	Data packetizing and buffering for logic components for integration into Velocia packet system.
Deframer	Parses Velocia packets and dissembles them.	Deframer is used to extract data payloads from packets for logic component integration into Velocia packet system.

IP for X6 Modules

ISI may provide upon request a range of up-conversion and down-conversion logic cores for wideband and narrowband receiver applications. FPGA-based FFT IP as well as chirp generation may also be available upon request. The X6 modules provide powerful receiver functionality integrated for IF processing with the addition of these optional cores. Contact ISI sales (ISIsales@molex.com) for more information.

The DDC channelizers are offered in channel densities from 4 to 256. The four channel DDC offers complete flexibility and independence in the channels, while the 128 and 256 channel cores offer higher density for uniform channel width applications. The DDC cores are highly configurable and include programmable channel filters, decimation rates, tuning and gain controls. An integrated power meter allows the DDC to measure any channel power for AGC controls. Multiple cores can be used for higher channel counts.

DDC Cores

Part Number	IP Core	Channels	Tuning	Decimation	Max Bandwidth	Channel Filter
58014	IP-MDDC4	4	Fs/2^32	16 to 32768	Fs/16	Programmable 100 tap filter
58015	IP-MDDC128	128	Fs/2^32	512 to 16384	Fs/512	Programmable 100 tap filter
58528	IP-DDC256	256	Fs/2^32	512 to 16384	Fs/512	Programmable 100 tap filter

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Signal processing cores for communications applications are optionally available for Virtex6. Contact ISI sales (ISIsales@molex.com) for more information.

Part Number	IP Core	Features
58001	PSK Demodulation	N=2,4,8,PI/4. Integrated carrier tracking and bit decision. Data rate to 160 Mbps.
58018	PSK Modulator	N=2,4,8,PI/4. Data rates up to 160 Mbps.
58002	FSK Demodulation	Coherent demodulation with carrier recovery,
58019	FSK Modulator	FSK modulation/
58020	QAM Modulator	Quadrature Amplitude Modulator.
58003	TinyDDS	Tiny DDS, 1/3 to ½ size of Xilinx DDS with equal SFDR, clock rates to 400 MHz with flow control
58011	XLFFT	IP core for 64K to 1M FFTs with windowing functions.
58012	Windowing	IP core for Hann, Blackman and uniform data windowing functions.
58013	CORDIC	IP core for sine/cosine generation using CORDIC method, resulting in 1/3 logic size of standard DDS cores.
58030	MDUC128	128-channel digital upconverter.

OFDM and LTE Cores

58029	OFDM Transmitter	OFDM transmit with IFFT, Windowing, Filtering, Cyclic Prefix and Upsample.
58031	OFDM Receiver	OFDM receiver with synchronization, downconversion and channel filtering.
58032	LTE Downlink Transmitter	LTE downlink transmitter core for FDD mode.
58033	LTE Uplink Receiver	LTE uplink receiver core for FDD mode includes 2K FFT, timing and frame synchronization using ML estimation method, decoding of SSS and PSS signals for cell ID and frame sync.

Applications Information

Cables

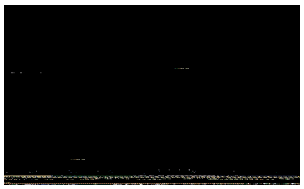
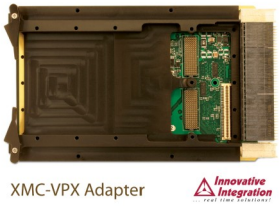
The X6-1000M module uses coaxial cable assemblies for the analog I/O. The mating cable should have an SSMC male connector and 50 ohm characteristic impedance for best signal quality.

XMC Adapter Boards

XMC modules can be used in standard desktop system or compact PCI/PXI using a XMC adapter board. An auxiliary power connector to the PCI Express adapters provides additional power capability for XMC modules when the slot is unable to provide sufficient power. The adapter boards allow the XMC modules to be used in any PCIe or PCI system.

The X6 module family uses the auxiliary XMC P16 connector as a private host interface. Eight high speed serial lanes with digital IO signals provide support for data transfer rates up to 4 GB/s sustained, as well as sideband signals for control and status. Protocols such as Aurora may be implemented for host communications or custom protocols.

X6-1000M

ASSY XMC-PCIe x8 ADAPTER (80363) x8 PCIe to XMC On-board USB to JTAG Programmer High speed expansion port (Mini-SAS, QSFP) Conduction Cooling External VPWR Power option available XMC Module Voltage and Current Test Header 	**PCIe-XMC Adapter (80341)** x8 PXIe to XMC Clock and trigger inputs 	**PCIe-XMC Adapter x8 lane (80259)** x8 PCIe to XMC P16 x8 RIO ports to SATA connectors Jn4 DIO to MDR68 Preferred for X6 	**PCIe-XMC Adapter x8 lane (80173)** x8 PCIe to XMC P16 x8 RIO ports to SATA2 connectors DIO to MDR68 
Compact PCI-XMC Adapter (80207) 64-bit, 133 MHz PCI-X host x4 PCIe to XMC PXI triggers and clock support 	**VPX-XMC Adapter (80260-0)** 3U conduction-cooled VPX adapter Configurable port A-D mapping Optional REDI covers 		

Applications that need remote or portable IO can use the eInstrument PC, VPXI-ePC or eInstrument Node with X6 modules.

X6-1000M

eInstrument PC with Dual PCI Express XMC Modules (90602) Windows/Linux embedded PC 8x USB, GbE, cable PCIe, VGA High speed x8 interconnect between modules GPS disciplined, programmable sample clocks and triggers to XMCs 2000 MB/s, 4 TB datalogger 9-18V operation	EPC-Nano (80342) Windows/Linux Embedded Single Board Computer Extremely small form-factor Single XMC IO Site and 1 GbE Link 8-14Vdc operation
	

X6-1000M

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